1. Record Nr. UNINA9910299745103321

Autore	Oh Taehyoun
Titolo	High performance multi-channel high-speed I/O circuits / / Taehyoun Oh, Ramesh Harjani
Pubbl/distr/stampa	New York : , : Springer, , 2014
ISBN	1-4614-4963-4
Edizione	[1st ed. 2014.]
Descrizione fisica	1 online resource (x, 89 pages) : illustrations (some color)
Collana	Analog Circuits and Signal Processing, , 1872-082X
Disciplina	621.3822
Soggetti	Signal processing Electronic circuit design Electromagnetic interference - Prevention Crosstalk - Prevention
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"ISSN: 1872-082X."
Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	Introduction -- 2x6 Gb/s MIMO Crosstalk Cancellation and Signal Reutilization Scheme in 130 nm CMOS Process -- 4x12 Gb/s MIMO Crosstalk Cancellation and Signal Reutilization Receiver in 65 nm CMOS Process -- Adaptive XTCR, AGC, and Adaptive DFE Loop -- Research Summary & Contributions -- References -- Appendix A: Noise Analysis -- Appendix B: Issues of Applying Consecutive 2x2 XTCR on Multi-Lane I/Os (4) -- Appendix C: Transmitter-Side Discrete-Time FIR XTC Filter versus Receiver-Side Analog-IIR XTC Filter -- Appendix D: Line Mismatch Sensitivity -- Appendix E: Input Matching for 4x4 XTCR Receiver Test Bench -- Appendix F: Bandwidth Improvement by Technology Scaling.
Sommario/riassunto	This book describes design techniques that can be used to mitigate crosstalk in high-speed I/O circuits. The focus of the book is in developing compact and low power integrated circuits for crosstalk cancellation, inter-symbol interference (ISI) mitigation and improved bit error rates (BER) at higher speeds. This book is one of the first to discuss in detail the problem of crosstalk and ISI mitigation encountered as data rates have continued beyond 10Gb/s. Readers will learn to avoid the data performance cliff, with circuits and design techniques described for novel, low power crosstalk cancellation

methods that are easily combined with current ISI mitigation architectures. · Describes technology and design ideas for power-efficient crosstalk cancellation in multi-channel high-speed I/O circuits; · Includes critical background knowledge related to channel ISI equalization circuits; · Provides crosstalk cancellation circuit methods that can be adapted efficiently to currently used equalization circuits in high-speed I/O receivers; key crosstalk cancellation blocks can be merged easily with automatic gain control (AGC) circuits in current I/O systems.