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| 1. Record Nr. | UNIORUON00406051 |
| Autore | Mingione, Enzo |
| Titolo | Occupazione, qualificazione e mercato del lavoro : una ricerca di qualificazione e l'occupazione impiegatizia in Italia oggi / Enzo Mingione, Francesca Zajczyk ; a cura di Istituto di sociologia. Università degli Studi di Milano |
| Pubbl/distr/stampa | Milano, : Sapere edizioni, 1974 |
| Descrizione fisica | 207 p. ; 20 cm. |
| Altri autori (Persone) | Zajczyk, Francesca |
| Soggetti | Sociologia del lavoro |
| Lingua di pubblicazione | Italiano |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| 2. Record Nr. | UNINA9910299666303321 |
| Titolo | Circuit Design for Reliability / / edited by Ricardo Reis, Yu Cao, Gilson Wirth |
| Pubbl/distr/stampa | New York, NY : , : Springer New York : , : Imprint : Springer, , 2015 |
| ISBN | 1-4614-4078-5 |
| Edizione | [1st ed. 2015.] |
| Descrizione fisica | 1 online resource (271 p.) |
| Disciplina | 620 620.00420285 621.3815 658.56 |
| Soggetti | Electronic circuits Security systems Computer-aided engineering Electronic Circuits and Systems Security Science and Technology Computer-Aided Engineering (CAD, CAE) and Design |
| Lingua di pubblicazione | Inglese |

| Formato | Materiale a stampa |
|-----------------------|---|
| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references at the end of each chapters. |
| Nota di contenuto | Introduction -- Recent Trends in Bias Temperature Instability -- Charge trapping phenomena in MOSFETS: From Noise to Bias Temperature Instability -- Atomistic Simulations on Reliability -- On-chip characterization of statistical device degradation -- Circuit Resilience Roadmap -- Layout Aware Electromigration Analysis of Power/Ground Networks -- Power-Gating for Leakage Control and Beyond -- Soft Error Rate and Fault Tolerance Techniques for FPGAs. |
| Sommario/riassunto | This book presents physical understanding, modeling and simulation, on-chip characterization, layout solutions, and design techniques that are effective to enhance the reliability of various circuit units. The authors provide readers with techniques for state of the art and future technologies, ranging from technology modeling, fault detection and analysis, circuit hardening, and reliability management. Provides comprehensive review on various reliability mechanisms at sub-45nm nodes; Describes practical modeling and characterization techniques for reliability; Includes thorough presentation of robust design techniques for major VLSI design units; Promotes physical understanding with first-principle simulations. |