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Titolo	Multi-Net Optimization of VLSI Interconnect [[electronic resource] /] / by Konstantin Moiseev, Avinoam Kolodny, Shmuel Wimer
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Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	An Overview of the VLSI Interconnect Problem -- Interconnect Aspects in Design Methodology and EDA Tools -- Scaling Dependent Electrical Modeling of Interconnects -- Net-by-Net Wire Optimization -- Multi-Net Sizing and Spacing of Bundle Wires -- Multi-net Sizing and Spacing in General Layouts -- Interconnect Optimization by Net Ordering -- Layout Migration -- Future Directions in Interconnect Optimization.
Sommario/riassunto	This book covers layout design and layout migration methodologies for optimizing multi-net wire structures in advanced VLSI interconnects. Scaling-dependent models for interconnect power, interconnect delay and crosstalk noise are covered in depth, and several design optimization problems are addressed, such as minimization of interconnect power under delay constraints, or design for minimal delay in wire bundles within a given routing area. A handy reference or

a guide for design methodologies and layout automation techniques, this book provides a foundation for physical design challenges of interconnect in advanced integrated circuits. • Describes the evolution of interconnect scaling and provides new techniques for layout migration and optimization, focusing on multi-net optimization; • Presents research results that provide a level of design optimization which does not exist in commercially-available design automation software tools; • Includes mathematical properties and conditions for optimality of layout, describes and analyses algorithmic solutions, and supplements analysis with examples taken from state-of-the-art chips. This book addresses an intriguing engineering challenge, namely the design of an enormous maze of wires, which run in about a dozen metal layers above billions of transistors in a modern processor. The physical insight, mathematical rigor and methodological approach described in the book, are essential for engineers and computer architects, as they develop new systems of ever-increasing complexity and migrate them to new generations of device technologies. The Authors of this book didn't only develop the academic methodologies, but actually developed CAD tools, and implemented their tools and methodologies to design VLSI chips. I had the privilege to work with them. --Mooly Eden, Senior Vice President, Intel Corporation; President, Intel Israel The speed, power, area, and reliability of high performance integrated circuits are determined by the on-chip interconnect. With the publication of this book, an important niche has been filled; that is local and global on-chip interconnect optimization. This book provides a theoretical basis for the practical design of the key issue in modern integrated circuits, the on-chip interconnect. --Eby G. Friedman, Distinguished Professor, University of Rochester.