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Titolo	Flip-Flop Design in Nanometer CMOS [[electronic resource]] : From High Speed to Low Energy / / by Massimo Alioto, Elio Consoli, Gaetano Palumbo
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Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	The Logical Effort Method -- Design in the Energy-Delay Space -- Clocked Storage Elements -- Flip-Flop Optimized Design -- Analysis and Comparison in the Energy-Delay-Area Domain -- Energy Efficiency Versus Clock Slope -- Hold Time Issues and Impact of variations on Flip-Flop Topologies -- Ultra-Fast and Energy-Efficient Pulsed Latch Topologies.
Sommario/riassunto	This book provides a unified treatment of Flip-Flop design and selection in nanometer CMOS VLSI systems. The design aspects related to the energy-delay tradeoff in Flip-Flops are discussed, including their energy-optimal selection according to the targeted application, and the detailed circuit design in nanometer CMOS VLSI systems. Design strategies are derived in a coherent framework that includes explicitly

nanometer effects, including leakage, layout parasitics and process/voltage/temperature variations, as main advances over the existing body of work in the field. The related design tradeoffs are explored in a wide range of applications and the related energy-performance targets. A wide range of existing and recently proposed Flip-Flop topologies are discussed. Theoretical foundations are provided to set the stage for the derivation of design guidelines, and emphasis is given on practical aspects and consequences of the presented results. Analytical models and derivations are introduced when needed to gain an insight into the inter-dependence of design parameters under practical constraints. This book serves as a valuable reference for practicing engineers working in the VLSI design area, and as text book for senior undergraduate, graduate and postgraduate students (already familiar with digital circuits and timing). • Provides a unified treatment of Flip-Flop design and energy/variation-aware selection in nanometer CMOS VLSI systems • Offers in-depth analysis of the impact of nanometer effects on design tradeoffs • Presents a comprehensive analysis, by considering more than 20 topologies covering all relevant classes of circuits • Uses a rigorous framework based on novel methodologies to include layout parasitics within the circuit design loop .