

1. Record Nr.	UNINA9910452023903321
Autore	Gordon Bernard <1918-2007.>
Titolo	The Gordon file [[electronic resource]] : a screenwriter recalls twenty years of FBI surveillance / / by Bernard Gordon
Pubbl/distr/stampa	Austin, : University of Texas Press, 2004
ISBN	0-292-79729-X
Edizione	[1st ed.]
Descrizione fisica	1 online resource (367 p.)
Disciplina	791.43/0232/092
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Soggetti	Screenwriters - United States Blacklisting of authors - United States Motion picture industry - United States Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Bernard Gordon filmography": p. [341]-344.

2. Record Nr.	UNINA9910299661303321
<b>Titolo</b>	Advanced Hardware Design for Error Correcting Codes / / edited by Cyrille Chavet, Philippe Coussy
<b>Pubbl/distr/stampa</b>	Cham : , : Springer International Publishing : , : Imprint : Springer, , 2015
<b>ISBN</b>	3-319-10569-8
<b>Edizione</b>	[1st ed. 2015.]
<b>Descrizione fisica</b>	1 online resource (197 p.)
<b>Disciplina</b>	005.7 620 621.3815 621.382
<b>Soggetti</b>	Electronic circuits Electrical engineering Computers Circuits and Systems Communications Engineering, Networks Information Systems and Communication Service
<b>Lingua di pubblicazione</b>	Inglese
<b>Formato</b>	Materiale a stampa
<b>Livello bibliografico</b>	Monografia
<b>Note generali</b>	Description based upon print version of record.
<b>Nota di bibliografia</b>	Includes bibliographical references.
<b>Nota di contenuto</b>	User Needs -- Challenges and Limitations for Very High Throughput Decoder Architectures for Soft-Decoding -- Implementation of Polar Decoders -- Parallel architectures for Turbo Product Codes Decoding -- VLSI implementations of sphere detectors -- Stochastic Decoders for LDPC Codes -- MP-SoC/NoC architectures for error correction -- ASIP design for multi-standard channel decoders -- Hardware design of parallel interleaver architecture: a survey.
<b>Sommario/riassunto</b>	This book provides thorough coverage of error correcting techniques. It includes essential basic concepts and the latest advances on key topics in design, implementation, and optimization of hardware/software systems for error correction. The book's chapters are written by internationally recognized experts in this field. Topics include evolution

of error correction techniques, industrial user needs, architectures, and design approaches for the most advanced error correcting codes (Polar Codes, Non-Binary LDPC, Product Codes, etc). This book provides access to recent results, and is suitable for graduate students and researchers of mathematics, computer science, and engineering. • Examines how to optimize the architecture of hardware design for error correcting codes; • Presents error correction codes from theory to optimized architecture for the current and the next generation standards; • Provides coverage of industrial user needs advanced error correcting techniques. Advanced Hardware Design for Error Correcting Codes includes a foreword by Claude Berrou.

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