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Sommario/riassunto	This book provides a comprehensive discussion of UML/OCL methods and design flow, for automatic validation and verification of hardware and software systems. While the presented flow focuses on using satisfiability solvers, the authors also describe how these methods can be used for any other automatic reasoning engine. Additionally, the design flow described is applied to a broad variety of validation and verification tasks. The authors also cover briefly how non-functional properties such as timing constraints can be handled with the described flow. Provides a general flow and description for the validation and verification of UML/OCL models; Demonstrates a detailed realization of the general flow using satisfiability solvers; Includes a case study that presents the possibilities of the state-of-the-art approaches.