1. Record Nr. UNINA9910299571203321

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Titolo	High-level Estimation and Exploration of Reliability for Multi-Processor System-on-Chip / / by Zheng Wang, Anupam Chattopadhyay
Pubbl/distr/stampa	Singapore : , : Springer Nature Singapore : , : Imprint : Springer, , 2018
ISBN	981-10-1073-0
Edizione	[1st ed. 2018.]
Descrizione fisica	1 online resource (XX, 197 p. 104 illus., 72 illus. in color.)
Collana	Computer Architecture and Design Methodologies, , 2367-3486
Disciplina	621.3815
Soggetti	Electronic circuits Computers Electronic Circuits and Systems Hardware Performance and Reliability
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	Introduction -- Background -- Related Work -- High-level Fault Injection and Simulation -- Architectural Reliability Estimation -- Architectural Reliability Exploration -- System-level Reliability Exploration -- Conclusion and Outlook.
Sommario/riassunto	This book introduces a novel framework for accurately modeling the errors in nanoscale CMOS technology and developing a smooth tool flow at high-level design abstractions to estimate and mitigate the effects of errors. The book presents novel techniques for high-level fault simulation and reliability estimation as well as architecture-level and system-level fault tolerant designs. It also presents a survey of state-of-the-art problems and solutions, offering insights into reliability issues in digital design and their cross-layer countermeasures. .