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Sommario/riassunto	This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge (ESD) protection. It is an invaluable reference for anyone developing systems-on-chip (SoC) and systems-on-package (SoP), integrated with system-level ESD protection. The book focuses on both the design of semiconductor integrated circuit (IC) components with embedded, on-chip system level protection and IC-system co-design. The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits, thereby reducing or completely eliminating the need for additional, discrete components on the printed circuit board (PCB) and meeting system-level ESD requirements. The authors

take a systematic approach, based on IC-system ESD protection co-design. A detailed description of the available IC-level ESD testing methods is provided, together with a discussion of the correlation between IC-level and system-level ESD testing methods. The IC-level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing. The overall methodology for IC-system ESD co-design is presented as a step-by-step procedure that involves both ESD testing and numerical simulations. • Provides a systematic approach for on-chip ESD protection design for system-level IC pins; • Describes a system-level co-design methodology, which uses external system level ESD protection components, together with on-chip ESD protection structure; • Includes a comprehensive description of wafer- level and component-level test methodologies and numerical simulations.