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Titolo	Design-for-test and test optimization techniques for TSV-based 3D stacked ICs / / Brandon Noia, Krishnendu Chakrabarty ; foreword by Vishwani Agrawal
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Nota di contenuto	Introduction -- Wafer Stacking and 3D Memory Test -- Built-in Self-Test for TSVs -- Pre-Bond TSV Test Through TSV Probing -- Pre-Bond TSV Test Through TSV Probing -- Overcoming the Timing Overhead of Test Architectures on Inter-Die Critical Paths -- Post-Bond Test Wrappers and Emerging Test Standards -- Test-Architecture Optimization and Test Scheduling -- Conclusions.
Sommario/riassunto	This book describes innovative techniques to address the testing needs of 3D stacked integrated circuits (ICs) that utilize through-silicon-vias (TSVs) as vertical interconnects. The authors identify the key challenges facing 3D IC testing and present results that have emerged from cutting-edge research in this domain. Coverage includes topics ranging from die-level wrappers, self-test circuits, and TSV probing to test-architecture design, test scheduling, and optimization. Readers will benefit from an in-depth look at test-technology solutions that are needed to make 3D ICs a reality and commercially viable. • Provides a comprehensive guide to the challenges and solutions for the testing of TSV-based 3D stacked ICs; • Includes in-depth explanation of key test and design-for-test technologies, emerging standards, and test-architecture and test-schedule optimizations; • Encompasses all

aspects of test as related to 3D ICs, including pre-bond and post-bond test as well as the test optimization and scheduling necessary to ensure that 3D testing remains cost-effective. .