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| | Autore | Mohammad Baker |
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| | Edizione | [1st ed. 2014.] |
| | Descrizione fisica | 1 online resource (xiii, 95 pages) : illustrations (chiefly color) |
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| | Soggetti | Embedded computer systems - Design and construction<br>Multiprocessors<br>Computer storage devices |
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| | Livello bibliografico | Monografia |
| | Note generali | "ISSN: 1872-082X."<br>"ISSN: 2197-1854 (electronic)." |
| | Nota di bibliografia | Includes bibliographical references. |
| | Nota di contenuto | Introduction -- Cache Architecture and Main Blocks -- Embedded Memory Hierarchy -- SRAM Memory Operation and Yield -- Low Power and High Yield SRAM Memory -- Leakage Reduction -- Embedded Memory Verification -- Embedded Memory Design Validation and Design For Test -- Emerging Memory Technology Opportunities and Challenges. |
| | Sommario/riassunto | This book describes the various tradeoffs systems designers face when designing embedded memory.  Readers designing multi-core systems and systems on chip will benefit from the discussion of different topics from memory architecture, array organization, circuit design techniques and design for test.  The presentation enables a multi-disciplinary approach to chip design, which bridges the gap between the architecture level and circuit level, in order to address yield, reliability and power-related issues for embedded memory. ·        Provides a comprehensive overview of embedded memory design and associated challenges and choices; ·        Explains tradeoffs and dependencies across different disciplines involved with multi-core and system on chip memory design; ·        Includes detailed discussion of memory hierarchy and its impact on energy and |

performance; ·      Uses real product examples to demonstrate embedded memory design flow from architecture, to circuit design, design for test and yield analysis.