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Nota di contenuto	Introduction -- Conventional Architecture of Turbo Decoder -- Turbo Decoder with Parallel Processing -- Low-Complexity Solution for Highly Parallel Architecture -- High Efficiency Solution for Highly Parallel Architecture.
Sommario/riassunto	This book describes the most recent techniques for turbo decoder implementation, especially for 4G and beyond 4G applications. The authors reveal techniques for the design of high-throughput decoders for future telecommunication systems, enabling designers to reduce hardware cost and shorten processing time. Coverage includes an explanation of VLSI implementation of the turbo decoder, from basic functional units to advanced parallel architecture. Several state-of-the-art techniques that improve complexity and/or throughput are introduced. The authors discuss both hardware architecture techniques and experimental results, showing the variations in area/throughput/performance with respect to several techniques. This book also illustrates turbo decoders for 3GPP-LTE/LTE-A and IEEE 802.16e/m standards, which provide a low-complexity but high-flexibility circuit structure to support these standards and enables

designs that reconfigure block size and parallelism. Case studies include the discussions of both throughput and performance of each mode (block size/parallelism/iteration). This book not only highlights the critical design issues that restrict the speedup of parallel architecture, but it also provides the solutions to overcome these limitations by modifying slightly the turbo codec of modern standards. · Offers readers a complete introduction to practical turbo decoder design; · Describes different design methodologies and explains the trade-offs between performance improvement and overhead; · Explains modern techniques for state-of-the-art designs; · Includes simulation and implementation results with respect to various decoder circuit designs; · Reveals novel approaches to higher operating efficiency of turbo decoders for beyond 4G applications.