

1. Record Nr.	UNINA9910299486003321
Titolo	Routing algorithms in networks-on-chip // Maurizio Palesi, Masoud Daneshtalab, editors
Pubbl/distr/stampa	New York : , : Springer, , 2014
ISBN	1-4614-8274-7
Edizione	[1st ed. 2014.]
Descrizione fisica	1 online resource (xiv, 410 pages) : illustrations (some color)
Collana	Gale eBooks
Disciplina	621.381531
Soggetti	Networks on a chip Computer algorithms
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Part I Performance Improvement -- Basic Concepts on On-Chip Networks -- A Heuristic Framework for Designing and Exploring Deterministic Routing Algorithm for NoCs -- Run-Time Deadlock Detection -- The Abacus Turn Model -- Learning-based Routing Algorithms for on-Chip Networks -- Part II Multicast Communication -- Efficient and Deadlock-Free Tree-based Multicast Routing Method for Network-on-Chip -- Path-based Multicast Routing for 2D and 3D Mesh Networks -- Part III Fault Tolerance and Reliability -- Fault-Tolerant Routing Algorithms in Networks-on-Chip -- Reliable and Adaptive Algorithms for 2D and 3D Networks-on-Chip.
Sommario/riassunto	This book provides a single-source reference to routing algorithms for Networks-on-Chip (NoCs), as well as in-depth discussions of advanced solutions applied to current and next generation, many core NoC-based Systems-on-Chip (SoCs). After a basic introduction to the NoC design paradigm and architectures, routing algorithms for NoC architectures are presented and discussed at all abstraction levels, from the algorithmic level to actual implementation. Coverage emphasizes the role played by the routing algorithm and is organized around key problems affecting current and next generation, many-core SoCs. A selection of routing algorithms is included, specifically designed to address key issues faced by designers in the ultra-deep sub-micron (UDSM) era, including performance improvement, power, energy, and thermal issues, fault tolerance and reliability. . Provides a

comprehensive overview of routing algorithms for Networks-on-Chip and NoC-based, manycore systems; · Describes routing algorithms for NoC architectures at all abstraction levels, from the algorithmic level to actual implementation; · Discusses the impact on NoC routing algorithms of key design objectives, such as power dissipation, energy consumption, thermal aspects, reliability, and performance.
