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Nota di contenuto	Introduction -- Digital Transmitter Architectures: Overview -- High-Level Analysis of Fully Digital PWM Transmitters -- Continuous-time Digital Design Techniques -- A 65-nm CMOS Fully Digital Reconfigurable Transmitter Front-End for Class-E PA based on Baseband PWM -- A 40-nm CMOS Fully Digital Reconfigurable Transmitter with Class-D Pas using Baseband and RF PWM -- Conclusions and Future Work.
Sommario/riassunto	This book describes the design of fully digital multistandard transmitter front-ends which can directly drive one or more switching power amplifiers, thus eliminating all other analog components. After reviewing different architectures, the authors focus on polar architectures using pulse width modulation (PWM), which are entirely based on unclocked delay lines and other continuous-time digital hardware. As a result, readers are enabled to shift accuracy concerns from the voltage domain to the time domain, to coincide with submicron CMOS technology scaling. The authors present different architectural options and compare them, based on their effect on the signal and spectrum quality. Next, a high-level theoretical analysis of two different PWM-based architectures – baseband PWM and RF PWM – is made. On the circuit level, traditional digital components and design techniques are revisited from the point of view of continuous-time digital circuits. Important design criteria are identified and different

solutions are presented, along with their advantages and disadvantages. Finally, two chips designed in nanometer CMOS technologies are described, along with measurement results for validation. · Describes the design of multistandard digital transmitters and/or continuous-time digital circuits, including theoretical models and adapted implementations of digital building blocks; · Uses a top-down approach, moving from the architectural level, via mathematical models and high-level simulations, down to circuit-level implementation aspects, including parasitic capacitances and variability; · Applies techniques described to the design of two Ghz-range multistandard transmitters.