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| Autore | Mandal Ayan |
| Titolo | Source-synchronous networks-on-chip : circuit and architectural interconnect modeling / / Ayan Mandal, Sunil P. Khatri, Rabi Mahapatra |
| Pubbl/distr/stampa | New York : , : Springer, , 2014 |
| ISBN | 1-4614-9405-2 |
| Edizione | [1st ed. 2014.] |
| Descrizione fisica | 1 online resource (xiii, 143 pages) : illustrations (some color) |
| Collana | Gale eBooks |
| Disciplina | 004.1<br>620<br>621.381<br>621.3815 |
| Soggetti | Networks on a chip - Design |
| Lingua di pubblicazione | Inglese |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Note generali | Includes index. |
| Nota di bibliografia | Includes bibliographical references and index. |
| Nota di contenuto | Introduction -- Clock Distribution for fast Networks-on-Chip -- Fast Network-on-Chip Design -- Fast On-Chip Data transfer using Sinusoid Signals -- Conclusion and Future Work. |
| Sommario/riassunto | This book describes novel methods for network-on-chip (NoC) design, using source-synchronous high-speed resonant clocks. The authors discuss NoCs from the bottom up, providing circuit level details, before providing architectural simulations. As a result, readers will get a complete picture of how a NoC can be designed and optimized. Using the methods described in this book, readers are enabled to design NoCs that are 5X better than existing approaches in terms of latency and throughput and can also sustain a significantly greater amount of traffic. • Describes novel methods for high-speed network-on-chip (NoC) design; • Enables readers to understand NoC design from both circuit and architectural levels; • Provides circuit-level details of the NoC (including clocking, router design), along with a high-speed, resonant clocking style which is used in the NoC; • Includes architectural simulations of the NoC, demonstrating significantly superior performance over the state-of-the-art. |