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	Nota di contenuto	An introduction to high-speed DRAM -- An I/O Line Configuration and Organization of DRAM -- Clock generation and distribution -- Transceiver Design -- TSV Interface for DRAM.
	Sommario/riassunto	This book provides an overview of recent advances in memory interface design at both the architecture and circuit levels. Coverage includes signal integrity and testing, TSV interface, high-speed serial interface including equalization, ODT, pre-emphasis, wide I/O interface including crosstalk, skew cancellation, and clock generation and distribution. Trends for further bandwidth enhancement are also covered. • Enables readers with minimal background in memory design to understand the basics of high-bandwidth memory interface design; • Presents state-of-the-art techniques for memory interface design; • Covers memory interface design at both the circuit level and system architecture level.