

1.	Record Nr.	UNISA990001247120203316
	Titolo	Deutsche Philologie im Aufriss : band III
	Pubbl/distr/stampa	Berlin, 1962
	Collocazione	II t B 377/3
	Lingua di pubblicazione	Tedesco
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Nota di contenuto	Helmut Arntz, Runenkunde, P.1849-1871. - Josef Oswald, Grundzuge der Katoholischen Kirchengeschichte, P. 1647-1728. - Werner Bergengruen, Erzahlende Prosa, P. 1429-1443.
2.	Record Nr.	UNISALENTO991000725889707536
	Autore	Olah, Vera
	Titolo	C2K : century 2 of KoMaL / [editor : Vera Olah]
	Pubbl/distr/stampa	Budapest : Roland Eotvos Physical Society, 1999
	ISBN	9638051825
	Edizione	[Preliminary ed]
	Descrizione fisica	160 p. : ill., map ; 22 cm.
	Classificazione	AMS 00A07 AMS 01A65
	Disciplina	510
	Soggetti	Mathematics-problems, exercises, etc Mathematics-study and teaching-Hungary
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	"1994-1997": Cover. Includes index

3. Record Nr.	UNINA9910293151803321
Autore	Rahman Rezaur
Titolo	Intel Xeon Phi coprocessor architecture and tools : the guide for application developers / / Rezaur Rahman
Pubbl/distr/stampa	Apress, 2013 New York : , : Apress, , 2013
ISBN	1-4302-5927-2
Edizione	[1st ed. 2013.]
Descrizione fisica	1 online resource (xxi, 209 pages) : illustrations (some color)
Collana	The expert's voice in microprocessors Gale eBooks
Disciplina	004 005.1
Soggetti	Coprocessors Computer programming High performance computing
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Includes index.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	""Contents at a Glance""; ""Contents""; ""About the Author""; ""About the Technical Reviewer""; ""Acknowledgments""; ""Introduction""; ""Part1: Hardware Foundation: Intel Xeon Phi Architecture""; ""Chapter 1: Introduction to Xeon Phi Architecture""; ""History of Intel Xeon Phi Development""; ""Evolution from Von Neumann Architecture to Cache Subsystem Architecture""; ""Improvements in the Core and Memory""; ""Instruction-Level Parallelism""; ""Instruction Pipelining""; ""Single Instruction Multiple Data""; ""Multithreading""; ""Multicore and Manycore Architecture"" ""Interconnect and Cache Improvements""""System Interconnect""; ""Intel Xeon Phi Coprocessor Chip Architecture""; ""Applicability of the Intel Xeon Phi Coprocessor""; ""Summary""; ""Chapter 2: Programming Xeon Phi""; ""Intel Xeon Phi Execution Models""; ""Development Tools for Intel Xeon Phi Architecture""; ""Intel Composer XE""; ""Getting the Tools""; ""Using the Compilers""; ""Setting Up an Intel Xeon Phi System""; ""Install the MPSS Stack""; ""Install the Development Tools""; ""Code Generation for Intel Xeon Phi Architecture""; ""Native Execution Mode""; ""Hello World Example""

""Language Extensions to Support Offload Computation on Intel Xeon Phi""
 ""Heterogeneous Computing Model and Offload Pragmas"";
 ""Language Extensions and Execution Model""; ""Terminology"";
 ""Offload Function and Data Declaration Directives""; ""declare target Directives""; ""Syntax""; ""C/C++""; ""Fortran""; ""Restrictions"";
 ""Function Offload and Execution Constructs""; ""Target Data Directive""; ""Syntax""; ""C/C++""; ""Fortran""; ""Restrictions""; ""Target Directive""; ""Syntax""; ""C/C++""; ""Fortran""; ""Restrictions""; ""Target Update Directive""; ""Syntax""; ""C/C++""; ""Fortran""
 ""Runtime Library Routines""""Offload Example""; ""Summary"";
 ""Chapter 3: Xeon Phi Vector Architecture and Instruction Set""; ""Xeon Phi Vector Microarchitecture""; ""The VPU Pipeline""; ""VPU Instruction Stalls""; ""Pairing Rule""; ""Vector Registers""; ""Vector Mask Registers""; ""Extended Math Unit""; ""Xeon Phi Vector Instruction Set Architecture""; ""Data Types""; ""Vector Nomenclature""; ""Vector Instruction Syntax""; ""Xeon Phi Vector ISA by Categories""; ""Mask Operations""; ""Swizzle, Shuffle, Broadcast, and Convert Instructions""; ""Swizzle""; ""Register Memory Swizzle""
 ""Data Broadcasts""""Data Conversions""; ""Shuffles""; ""Shift Operation""; ""Logical Shifts""; ""Arithmetic Shifts""; ""Sample Code for Swizzle and Shuffle Instructions""; ""Arithmetic and Logic Operations""; ""Fused Multiply-Add""; ""Data Access Operations (Load, Store, Prefetch, and Gather/Scatter)""; ""Memory Alignment""; ""Pack/ U npack""; ""Non-temporal data""; ""Streaming Stores""; ""Scatter/Gather""; ""Prefetch Instructions""; ""Summary""; ""Chapter 4: Xeon Phi Core Microarchitecture""; ""Intel Xeon Phi Cores""; ""Core Pipeline Stages""; ""Cache and TLB Structure""
 ""L2 Cache Structure""

Sommario/riassunto

Intel® Xeon Phi™ Coprocessor Architecture and Tools: The Guide for Application Developers provides developers a comprehensive introduction and in-depth look at the Intel Xeon Phi coprocessor architecture and the corresponding parallel data structure tools and algorithms used in the various technical computing applications for which it is suitable. It also examines the source code-level optimizations that can be performed to exploit the powerful features of the processor. Xeon Phi is at the heart of world's fastest commercial supercomputer, which thanks to the massively parallel computing capabilities of Intel Xeon Phi processors coupled with Xeon Phi coprocessors attained 33.86 teraflops of benchmark performance in 2013. Extracting such stellar performance in real-world applications requires a sophisticated understanding of the complex interaction among hardware components, Xeon Phi cores, and the applications running on them. In this book, Rezaur Rahman, an Intel leader in the development of the Xeon Phi coprocessor and the optimization of its applications, presents and details all the features of Xeon Phi core design that are relevant to the practice of application developers, such as its vector units, hardware multithreading, cache hierarchy, and host-to-coprocessor communication channels. Building on this foundation, he shows developers how to solve real-world technical computing problems by selecting, deploying, and optimizing the available algorithms and data structure alternatives matching Xeon Phi's hardware characteristics. From Rahman's practical descriptions and extensive code examples, the reader will gain a working knowledge of the Xeon Phi vector instruction set and the Xeon Phi microarchitecture whereby cores execute 512-bit instruction streams in parallel.