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Nota di contenuto	Verification of Systems -- Introduction to Formal Verification of SystemC Models -- Symbolic Model Checking with Partial Order Reduction -- Efficient Symbolic State Matching using State Subsumption -- Heuristic Approaches for Symbolic State Matching -- Evaluation of Proposed Techniques.
Sommario/riassunto	In his master thesis, Vladimir Herdt presents a novel approach, called complete symbolic simulation, for a more efficient verification of much larger (non-terminating) SystemC programs. The approach combines symbolic simulation with stateful model checking and allows to verify safety properties in (cyclic) finite state spaces, by exhaustive exploration of all possible inputs and process schedulings. The state explosion problem is alleviated by integrating two complementary reduction techniques. Compared to existing approaches, the complete symbolic simulation works more efficiently, and therefore can provide correctness proofs for larger systems, which is one of the most challenging tasks, due to the ever increasing complexity. Contents Verification of Systems Introduction to Formal Verification of SystemC

Models Symbolic Model Checking with Partial Order Reduction Efficient
Symbolic State Matching using State Subsumption Heuristic Approaches
for Symbolic State Matching Evaluation of Proposed Techniques Target
Groups Lecturers and Students of Computer Sciences and Electrical
Engineering Hardware Designers and Verification Engineers using
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