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Nota di bibliografia	Includes bibliographical references.
Nota di contenuto	1 Introduction and Overview -- 2 Understanding of Process-Induced Random Variation -- 3 Various Variation-Robust CMOS Device Designs -- 4 Applications to Static Random Access Memory (SRAM) -- 5 Conclusion.
Sommario/riassunto	This book provides a comprehensive overview of contemporary issues in complementary metal-oxide semiconductor (CMOS) device design, describing how to overcome process-induced random variations such as line-edge-roughness, random-dopant-fluctuation, and work-function variation, and the applications of novel CMOS devices to cache memory (or Static Random Access Memory, SRAM). The author places emphasis on the physical understanding of process-induced random variation as well as the introduction of novel CMOS device structures and their application to SRAM. The book outlines the technical predicament facing state-of-the-art CMOS technology development, due to the effect of ever-increasing process-induced random/intrinsic variation in transistor performance at the sub-30-nm technology nodes. Therefore, the physical understanding of process-induced

random/intrinsic variations and the technical solutions to address these issues plays a key role in new CMOS technology development. This book aims to provide the reader with a deep understanding of the major random variation sources, and the characterization of each random variation source. Furthermore, the book presents various CMOS device designs to surmount the random variation in future CMOS technology, emphasizing the applications to SRAM.

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