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Autore	Wang Ran
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Nota di bibliografia	Includes bibliographical references at the end of each chapters.
Nota di contenuto	Introduction -- Pre-Bond Testing of the Silicon Interposer -- Post-Bond Scan-based Testing of Interposer Interconnects -- Test Architecture and Test-Path Scheduling -- Built-In Self-Test -- ExTest Scheduling and Optimization -- A Programmable Method for Low-Power Scan Shift in SoC Dies -- Conclusions.-.
Sommario/riassunto	This book provides readers with an insightful guide to the design, testing and optimization of 2.5D integrated circuits. The authors describe a set of design-for-test methods to address various challenges posed by the new generation of 2.5D ICs, including pre-bond testing of the silicon interposer, at-speed interconnect testing, built-in self-test architecture, extest scheduling, and a programmable method for low-power scan shift in SoC dies. This book covers many testing techniques that have already been used in mainstream semiconductor companies. Readers will benefit from an in-depth look at test-technology solutions that are needed to make 2.5D ICs a reality and commercially viable. Provides a single-source guide to the practical challenges in testing of 2.5D ICs; Presents an efficient method to locate

defects in a passive interposer before stacking; Describes an efficient interconnect-test solution to target through-silicon vias (TSVs), the redistribution layer, and micro-bumps for shorts, opens, and delay faults; Provides a built-in self-test (BIST) architecture that can be enabled by the standard TAP controller in the IEEE 1149.1 standard; Discusses two ExTest scheduling strategies to implement interconnect testing between tiles inside an SoC die; Includes a programmable method for shift-clock stagger assignment to reduce power supply noise during SoC die testing in 2.5D ICs.