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Titolo	Rural gender studies in Europe / Leendert van der Plas, Maria Fonte (eds)
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2. Record Nr.	UNINA9910254237603321
Autore	Spiridon Silvian
Titolo	Toward 5G Software Defined Radio Receiver Front-Ends / / by Silvian Spiridon
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Descrizione fisica	1 online resource (XVII, 96 p. 50 illus., 20 illus. in color.)
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Soggetti	Electronic circuits Signal processing Image processing Speech processing systems Electronics Microelectronics Circuits and Systems Signal, Image and Speech Processing Electronics and Microelectronics, Instrumentation
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Nota di bibliografia	Includes bibliographical references at the end of each chapters.
Nota di contenuto	Overview of Wireless Communication in the Internet Age -- Defining the optimal architecture -- From High Level Standard Requirements to Circuit Level Electrical Specifications: A Standard Independent Approach -- Optimal Filter Partitioning -- Smart Gain Partitioning for Noise -- Linearity Trade-Off Optimization -- SDRX Electrical Specifications -- A System Level Perspective of Modern Receiver Building Blocks -- Conclusions and Future Developers.
Sommario/riassunto	This book introduces a new intuitive design methodology for the optimal design path for next-generation software defined radio front-ends (SDRXs). The methodology described empowers designers to "attack" the multi-standard environment in a parallel way rather than serially, providing a critical tool for any design methodology targeting 5G circuits and systems. Throughout the book the SDRX design follows the key wireless standards of the moment (i.e., GSM, WCDMA, LTE, Bluetooth, WLAN), since a receiver compatible with these standards is the most likely candidate for the first design iteration in a 5G deployment. The author explains the fundamental choice the designer has to make regarding the optimal channel selection: how much of the blockers/interferers will be filtered in the analog domain and how much will remain to be filtered in the digital domain. The system-level analysis the author describes entails the direct sampling architecture is treated as a particular case of mixer-based direct conversion architecture. This allows readers give a power consumption budget to determine how much filtering is required on the receive path, by considering the ADC performance characteristics and the corresponding blocker diagram.