

1. Record Nr.	UNINA9910254218503321
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Titolo	Digital Logic Design Using Verilog : Coding and RTL Synthesis // by Vaibhav Taraate
Pubbl/distr/stampa	New Delhi : , : Springer India : , : Imprint : Springer, , 2016
ISBN	81-322-2791-3
Edizione	[1st ed. 2016.]
Descrizione fisica	1 online resource (431 p.)
Disciplina	620
Soggetti	Electronic circuits Electronics Microelectronics Logic design Circuits and Systems Electronics and Microelectronics, Instrumentation Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Introduction -- Combinational Logic Design (Part I) -- Combinational Logic Design (Part II) -- Combinational Design Guidelines -- Sequential Logic Design -- Sequential Design Guidelines -- Complex Designs using Verilog RTL -- Finite State Machines -- Simulation Concepts and PLD Based Designs -- RTL Synthesis -- Static Timing Analysis (STA) -- Constraining Design -- Multiple Clock Domain Designs -- Low Power Design -- RTL Design for SOCs.
Sommario/riassunto	This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also

describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists. .
