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Autore	Barkalov Alexander
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Nota di contenuto	Preface; Contents; Abbreviations; 1 Background of Finite State Machines and Programmable Logic; 1.1 Basic Models of FSMs; 1.2 Logic Synthesis for Microprogram Automata; 1.3 Logic Synthesis for Microprogram Control Units; 1.4 Logic Synthesis for Compositional MCUs; 1.5 Hardware Reduction for FPLD-Based FSMs; References; 2 Field Programmable Gate Arrays in FSM Design; 2.1 General Characteristic of FPGAs; 2.2 Trivial Implementing FPGA-Based FSMs; 2.3 Methods of State Assignment; 2.4 Hardware Reduction for FPGA-Based FSMs; References; 3 Object Codes Transformation for Mealy FSMs; 3.1 Principle of OCT for Mealy FSMs; 3.2 Synthesis of FPGA-Based Mealy FSMs with Transformation of States; 3.3 Synthesis of FPGA-Based Mealy FSMs with Transformation of CMOs; 3.4 Replacement of Logical Conditions in Mealy FSMs with OCT; 3.5 Analysis of Proposed Methods; References; 4 Object Codes Transformation for Moore FSMs; 4.1 Principle of OCT for Moore FSMs; 4.2 Synthesis of FPGA-Based Moore FSMs with Transformations of States; 4.3 Synthesis of FPGA-Based

Moore FSMs with Transformation of CMOs; 4.4 Replacement of Logical Conditions in Moore FSMs with OCT; References

5 Distribution of Class Codes in Moore FSMs; 5.1 The Case of CPLD-Based FSMs; 5.2 Two Sources of Class Codes in FPGA-Based Moore FSMs; 5.3 Three Sources of Class Codes in FPGA-Based Moore FSMs; 5.4 Replacement of Logical Conditions and Distribution of Class Codes; 5.5 Increasing the Number of Class Variables; References; 6 Hardware Reduction in Multidirectional Moore FSMs; 6.1 Hardware Reduction in Two-Directional Moore FSMs; 6.2 Hardware Reduction in 3-Directional Moore FSMs; 6.3 Replacement of Logical Conditions for K-Directional Moore FSMs; References; 7 Design of EMB-Based Mealy FSMs

7.1 Trivial Implementing Mealy FSMs; 7.2 Encoding of Objects in Mealy FSMs; 7.3 Replacement of Logical Conditions for Mealy FSMs; 7.4 Hardware Reduction for BRLC; References; 8 Design of EMB-Based Moore FSMs; 8.1 Trivial Implementing Moore FSMs; 8.2 Structural Decomposition for Moore FSMs; 8.3 Optimization of BIMF Based on Pseudoequivalent States; 8.4 Optimizing LUTer in Replacement of Logical Conditions; References; Conclusion; Index

Sommario/riassunto

This book discusses control units represented by the model of a finite state machine (FSM). It contains various original methods and takes into account the peculiarities of field-programmable gate arrays (FPGA) chips and a FSM model. It shows that one of the peculiarities of FPGA chips is the existence of embedded memory blocks (EMB). The book is devoted to the solution of problems of logic synthesis and reduction of hardware amount in control units. The book will be interesting and useful for researchers and PhD students in the area of Electrical Engineering and Computer Science, as well as for designers of modern digital systems.
