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7.1 Trivial Implementing Mealy FSMs7.2 Encoding of Objects in Mealy FSMs; 7.3 Replacement of Logical Conditions for Mealy FSMs; 7.4 Hardware Reduction for BRLC; References; 8 Design of EMB-Based Moore FSMs; 8.1 Trivial Implementing Moore FSMs; 8.2 Structural Decomposition for Moore FSMs; 8.3 Optimization of BIMF Based on Pseudoequivalent States; 8.4 Optimizing LUTer in Replacement of Logical Conditions; References; Conclusion; Index

Sommario/riassunto

This book discusses control units represented by the model of a finite state machine (FSM). It contains various original methods and takes into account the peculiarities of field-programmable gate arrays (FPGA) chips and a FSM model. It shows that one of the peculiarities of FPGA chips is the existence of embedded memory blocks (EMB). The book is devoted to the solution of problems of logic synthesis and reduction of hardware amount in control units. The book will be interesting and useful for researchers and PhD students in the area of Electrical Engineering and Computer Science, as well as for designers of modern digital systems.