| Record Nr. | UNINA9910254193103321 |
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| Titolo | Near Threshold Computing : Technology, Methods and Applications / / edited by Michael Hübner, Cristina Silvano |
| Pubbl/distr/stampa | Cham : , : Springer International Publishing : , : Imprint : Springer, , 2016 |
| ISBN | 3-319-23389-0 |
| Edizione | [1st ed. 2016.] |
| Descrizione fisica | 1 online resource (104 p.) |
| Disciplina | 620 |
| Soggetti | Electronic circuits |
| | Microprocessors |
| | Circuits and Systems |
| | Processor Architectures Electronic Circuits and Devices |
| | |
| Lingua di pubblicazione | |
| Formato | Materiale a stampa |
| Livello bibliografico | Monografia |
| Note generali | Description based upon print version of record. |
| Nota di bibliografia | Includes bibliographical references. |
| Nota di contenuto | PART I: NTC opportunities, challenges and limits Chapter 1: Extreme Energy Efficiency by Near Threshold Voltage Operation Part II Micro- architecture challenges and energy management at NTC Chapter2: Many-core Architecture for NTC: Energy Efficiency from the Ground Up Chapter 3: Variability-Aware Voltage Island Management for Near- Threshold Voltage Computing With Performance Guarantees Part III Memory system design for NTC Chapter4: Resizable Data Composer (RDC) Cache: A Near-Threshold Cache tolerating Process Variation Via architectural fault tolerance Chapter 5 Memories for NTC. |
| Sommario/riassunto | This book explores near-threshold computing (NTC), a design-space using techniques to run digital chips (processors) near the lowest possible voltage. Readers will be enabled with specific techniques to design chips that are extremely robust; tolerating variability and resilient against errors. Variability-aware voltage and frequency allocation schemes will be presented that will provide performance guarantees, when moving toward near-threshold manycore chips. Provides an introduction to near-threshold computing, enabling reader with a variety of tools to face the challenges of the |

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power/utilization wall; Demonstrates how to design efficient voltage regulation, so that each region of the chip can operate at the most efficient voltage and frequency point; Investigates how performance guarantees can be ensured when moving towards NTC manycores through variability-aware voltage and frequency allocation schemes.