1. Record Nr. UNINA9910254184203321

Autore	Palchaudhuri Ayan
Titolo	High Performance Integer Arithmetic Circuit Design on FPGA [[electronic resource]] : Architecture, Implementation and Design Automation / / by Ayan Palchaudhuri, Rajat Subhra Chakraborty
Pubbl/distr/stampa	New Delhi : , : Springer India : , : Imprint : Springer, , 2016
ISBN	81-322-2520-1
Edizione	[1st ed. 2016.]
Descrizione fisica	1 online resource (125 p.)
Collana	Springer Series in Advanced Microelectronics, , 1437-0387 ; ; 51
Disciplina	621.395
Soggetti	Electronic circuits Electronics Microelectronics Logic design Circuits and Systems Electronics and Microelectronics, Instrumentation Logic Design
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Introduction -- Architecture of Target FPGA Platform -- A Fabric Component based Design Approach for High Performance Integer Arithmetic Circuits -- Architecture of Data path Circuits -- Architecture of Control path Circuits -- Compact FPGA Implementation of Linear Cellular Automata -- Design Automation and Case Studies -- Conclusions and Future Work.
Sommario/riassunto	This book describes the optimized implementations of several arithmetic datapath, controlpath and pseudorandom sequence generator circuits for realization of high performance arithmetic circuits targeted towards a specific family of the high-end Field Programmable Gate Arrays (FPGAs). It explores regular, modular, cascadable, and bit-sliced architectures of these circuits, by directly instantiating the target FPGA-specific primitives in the HDL. Every proposed architecture is justified with detailed mathematical analyses. Simultaneously, constrained placement of the circuit building blocks is

	performed, by placing the logically related hardware primitives in close proximity to one another by supplying relevant placement constraints in the Xilinx proprietary “User Constraints File”. The book covers the implementation of a GUI-based CAD tool named FlexiCore integrated with the Xilinx Integrated Software Environment (ISE) for design automation of platform-specific high-performance arithmetic circuits from user-level specifications. This tool has been used to implement the proposed circuits, as well as hardware implementations of integer arithmetic algorithms where several of the proposed circuits are used as building blocks. Implementation results demonstrate higher performance and superior operand-width scalability for the proposed circuits, with respect to implementations derived through other existing approaches. This book will prove useful to researchers, students, and professionals engaged in the domain of FPGA circuit optimization and implementation.

2.

Record Nr.	UNISALENTO991004138969707536
Autore	Dallera, Giuseppe
Titolo	Autonomie locali e tributi / di Giuseppe Dallera, Marco Boccaccio e Guido Stazi
Pubbl/distr/stampa	Roma : Fondazione Luigi Einaudi per studi di politica ed economia, 1990
Descrizione fisica	185 p. ; 21 cm
Collana	Quaderni
Altri autori (Persone)	Boccaccio, Marcoauthor Stazi, Guido
Disciplina	336.014
Soggetti	Enti locali - Autonomia tributaria - Italia
Lingua di pubblicazione	Italiano
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Bibliografia: p. 181-185