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Nota di bibliografia	Includes bibliographical references at the end of each chapters.
Nota di contenuto	1. Introduction -- 2. IP Cores Design from Specifications to Production: Modeling, Verification, Optimization, and Protection -- 3. Analyzing the Trade-off between Different Memory Cores and Controllers -- 4. SOC BUSES AND PERIPHERALS: FEATURES AND ARCHITECTURES -- 5. Verilog for Implementation and Verification -- 6. New Trends in SoC Verification: UVM, Bug Localization, Scan-Chain-Based Methodology, GA-Based Test Generation -- 7. Conclusions.
Sommario/riassunto	This book describes the life cycle process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection. Various trade-offs in the design process are discussed, including those associated with many of the most common memory cores, controller IPs and system-on-chip (SoC) buses. Readers will also benefit from the author's practical coverage of new verification methodologies. such as bug localization, UVM, and scan-chain. A SoC case study is presented to compare traditional verification with the new verification methodologies. · Discusses the entire life cycle

process of IP cores, from specification to production, including IP modeling, verification, optimization, and protection; · Introduce a deep introduction for Verilog for both implementation and verification point of view. · Demonstrates how to use IP in applications such as memory controllers and SoC buses. · Describes a new verification methodology called bug localization; · Presents a novel scan-chain methodology for RTL debugging; · Enables readers to employ UVM methodology in straightforward, practical terms.