

1. Record Nr.	UNINA9910157536603321
Autore	Omura Y (Yasuhisa)
Titolo	MOS devices for low-voltage and low-energy applications // Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo
Pubbl/distr/stampa	Singapore ; ; Hoboken, NJ : , : John Wiley & Sons, , 2017 [Piscataway, New Jersey] : , : IEEE Xplore, , [2016]
ISBN	1-5231-1527-0 1-119-10738-5 1-119-10736-9
Descrizione fisica	1 online resource (758 pages) : illustrations, tables, graphs
Disciplina	621.3815/284
Soggetti	Metal oxide semiconductors Metal oxide semiconductor field-effect transistors Low voltage integrated circuits Low voltage systems - Industrial applications
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
Nota di contenuto	Preface XV -- Acknowledgments Xvi -- Part I Introduction To Low Voltage And Low Energy Devices 1 -- 1 Why Are Low Voltage And Low Energy Devices Desired? 3 -- References 4 -- 2 History Of Low Voltage And Low Power Devices 5 -- 2.1 Scaling Scheme And Low Voltage Requests 5 -- 2.2 Silicon On Insulator Devices And Real History 8 -- References 10 -- 3 Performance Prospects Of Subthreshold Logic Circuits 12 -- 3.1 Introduction 12 -- 3.2 Subthreshold Logic And Its Issues 12 -- 3.3 Is Subthreshold Logic The Best Solution? 13 -- References 13 -- Part Ii Summary Of Physics Of Modern Semiconductor Devices 15 -- 4 Overview 17 -- References 18 -- 5 Bulk Mosfet 19 -- 5.1 Theoretical Basis Of Bulk Mosfet Operation 19 -- 5.2 Subthreshold Characteristics: "Boff State" 19 -- 5.2.1 Fundamental Theory 19 -- 5.2.2 Influence Of Btbt Current 23 -- 5.2.3 Points To Be Remarkd 24 -- 5.3 Post Threshold Characteristics: "Bon State" 24 -- 5.3.1 Fundamental Theory 24 -- 5.3.2 Self Heating Effects 26 -- 5.3.3 Parasitic Bipolar Effects 27 -- 5.4 Comprehensive Summary Of Short

Channel Effects 27 -- References 28 -- 6 Soi Mosfet 29 -- 6.1 Partially Depleted Silicon On Insulator Metal Oxide Semiconductor Field Effect Transistors 29 -- 6.2 Fully Depleted (Fd) Soi Mosfet 30 -- 6.2.1 Subthreshold Characteristics 30 -- 6.2.2 Post Threshold Characteristics 36 -- 6.2.3 Comprehensive Summary Of Short Channel Effects 41 -- 6.3 Accumulation Mode (Am) Soi Mosfet 41 -- 6.3.1 Aspects Of Device Structure 41 -- 6.3.2 Subthreshold Characteristics 42 -- 6.3.3 Drain Current Component (I) Body Current (Id,Body) 43 -- 6.3.4 Drain Current Component (Ii) Surface Accumulation -- Layer Current (Id,Acc) 45 -- 6.3.5 Optional Discussions On The Accumulation Mode Soi Mosfet 45 -- 6.4 Finfet And Triple Gate Fet 46 -- 6.4.1 Introduction 46 -- 6.4.2 Device Structures And Simulations 46 -- 6.4.3 Results And Discussion 47 -- 6.4.4 Summary 49 -- 6.5 Gate All Around Mosfet 50 -- References 51 -- 7 Tunnel Field Effect Transistors (Tfets) 53. 7.1 Overview 53 -- 7.2 Model of Double Gate Lateral Tunnel FET and Device Performance Perspective 53 -- 7.2.1 Introduction 53 -- 7.2.2 Device Modeling 54 -- 7.2.3 Numerical Calculation Results and Discussion 61 -- 7.2.4 Summary 65 -- 7.3 Model of Vertical Tunnel FET and Aspects of its Characteristics 65 -- 7.3.1 Introduction 65 -- 7.3.2 Device Structure and Model Concept 65 -- 7.3.3 Comparing Model Results with TCAD Results 69 -- 7.3.4 Consideration of the Impact of Tunnel Dimensionality on Drivability 72 -- 7.3.5 Summary 75 -- 7.4 Appendix Integration of Eqs. (7.14) / (7.16) 76 -- References 78 -- Part III POTENTIAL OF CONVENTIONAL BULK MOSFETs 81 -- 8 Performance Evaluation of Analog Circuits with Deep Submicrometer MOSFETs in the Subthreshold Regime of Operation 83 -- 8.1 Introduction 83 -- 8.2 Subthreshold Operation and Device Simulation 84 -- 8.3 Model Description 85 -- 8.4 Results 86 -- 8.5 Summary 90 -- References 90 -- 9 Impact of Halo Doping on the Subthreshold Performance of Deep Submicrometer CMOS Devices and Circuits for Ultralow Power Analog/Mixed Signal Applications 91 -- 9.1 Introduction 91 -- 9.2 Device Structures and Simulation 92 -- 9.3 Subthreshold Operation 93 -- 9.4 Device Optimization for Subthreshold Analog Operation 95 -- 9.5 Subthreshold Analog Circuit Performance 98 -- 9.6 CMOS Amplifiers with Large Geometry Devices 105 -- 9.7 Summary 106 -- References 107 -- 10 Study of the Subthreshold Performance and the Effect of Channel Engineering on Deep Submicron Single Stage CMOS Amplifiers 108 -- 10.1 Introduction 108 -- 10.2 Circuit Description 108 -- 10.3 Device Structure and Simulation 110 -- 10.4 Results and Discussion 110 -- 10.5 PTAT as a Temperature Sensor 116 -- 10.6 Summary 116 -- References 116 -- 11 Subthreshold Performance of Dual Material Gate CMOS Devices and Circuits for Ultralow Power Analog/Mixed Signal Applications 117 -- 11.1 Introduction 117 -- 11.2 Device Structure and Simulation 118 -- 11.3 Results and Discussion 120 -- 11.4 Summary 126. References 127 -- 12 Performance Prospect of Low Power Bulk MOSFETs 128 -- Reference 129 -- Part IV POTENTIAL OF FULLY DEPLETED SOI MOSFETs 131 -- 13 Demand for High Performance SOI Devices 133 -- 14 Demonstration of 100 nm Gate SOI CMOS with a Thin Buried Oxide Layer and its Impact on Device Technology 134 -- 14.1 Introduction 134 -- 14.2 Device Design Concept for 100 nm Gate SOI CMOS 134 -- 14.3 Device Fabrication 136 -- 14.4 Performance of 100 nm and 85 nm Gate Devices 137 -- 14.4.1 Threshold and Subthreshold Characteristics 137 -- 14.4.2 Drain Current (ID) Drain Voltage (VD) and ID Gate Voltage (VG) Characteristics of 100 nm Gate MOSFET/SIMOX 138 -- 14.4.3 ID / VD

and ID / VG Characteristics of 85nm Gate MOSFET/SIMOX 142 -- 14.4.4 Switching Performance 142 -- 14.5 Discussion 142 -- 14.5.1 Threshold Voltage Balance in Ultrathin CMOS/SOI Devices 142 -- 14.6 Summary 144 -- References 145 -- 15 Discussion on Design Feasibility and Prospect of High Performance Sub-50 nm Channel Single Gate SOI MOSFET Based on the ITRS Roadmap 147 -- 15.1 Introduction 147 -- 15.2 Device Structure and Simulations 148 -- 15.3 Proposed Model for Minimum Channel Length 149 -- 15.3.1 Minimum Channel Length Model Constructed using Extract A 149 -- 15.3.2 Minimum Channel Length Model Constructed using Extract B 150 -- 15.4 Performance Prospects of Scaled SOI MOSFETs 152 -- 15.4.1 Dynamic Operation Characteristics of Scaled SG SOI MOSFETs 152 -- 15.4.2 Tradeoff and Optimization of Standby Power Consumption and Dynamic Operation 157 -- 15.5 Summary 162 -- References 162 -- 16 Performance Prospects of Fully Depleted SOI MOSFET Based Diodes Applied to Schenkel Circuits for RF/ID Chips 164 -- 16.1 Introduction 164 -- 16.2 Remaining Issues with Conventional Schenkel Circuits and an Advanced Proposal 165 -- 16.3 Simulation Based Consideration of RF Performance of SOI/QD 172 -- 16.4 Summary 176 -- 16.5 Appendix: A Simulation Model for Minority Carrier Lifetime 177 -- 16.6 Appendix: Design Guideline for SOI/QDs 177. References 178 -- 17 The Potential and the Drawbacks of Underlap Single Gate Ultrathin SOI MOSFET 180 -- 17.1 Introduction 180 -- 17.2 Simulations 181 -- 17.3 Results and Discussion 183 -- 17.3.1 DC Characteristics and Switching Performance: Device A 183 -- 17.3.2 RF Analog Characteristics: Device A 184 -- 17.3.3 Impact of High Gate Dielectric on Performance of USU SOI MOSFET Devices: Devices B and C 185 -- 17.3.4 Impact of Simulation Model on Simulation Results 189 -- 17.4 Summary 192 -- References 192 -- 18 Practical Source/Drain Diffusion and Body Doping Layouts for High Performance and Low Energy Triple Gate SOI MOSFETs 194 -- 18.1 Introduction 194 -- 18.2 Device Structures and Simulation Model 195 -- 18.3 Results and Discussion 196 -- 18.3.1 Impact of S/D Underlying Layer on ION, IOFF, and Subthreshold Swing 196 -- 18.3.2 Tradeoff of Short Channel Effects and Drivability 196 -- 18.4 Summary 201 -- References 201 -- 19 Gate Field Engineering and Source/Drain Diffusion Engineering for High Performance Si Wire Gate All Around MOSFET and Low Power Strategy in a Sub-30 nm Channel Regime 203 -- 19.1 Introduction 203 -- 19.2 Device Structures Assumed and Physical Parameters 204 -- 19.3 Simulation Results and Discussion 206 -- 19.3.1 Performance of Sub-30 nm Channel Devices and Aspects of Device Characteristics 206 -- 19.3.2 Impact of Cross Section of Si Wire on Short Channel Effects and Drivability 212 -- 19.3.3 Minimizing Standby Power Consumption of GAA SOI MOSFET 216 -- 19.3.4 Prospective Switching Speed Performance of GAA SOI MOSFET 217 -- 19.3.5 Parasitic Resistance Issues of GAA Wire MOSFETs 218 -- 19.3.6 Proposal for Possible GAA Wire MOSFET Structure 220 -- 19.4 Summary 221 -- 19.5 Appendix: Brief Description of Physical Models in Simulations 221 -- References 225 -- 20 Impact of Local High Insulator on Drivability and Standby Power of Gate All Around SOI MOSFET 228 -- 20.1 Introduction 228 -- 20.2 Device Structure and Simulations 229 -- 20.3 Results and Discussion 230. 20.3.1 Device Characteristics of GAA Devices with Graded

Profile Junctions 230 -- 20.3.2 Device Characteristics of GAA Devices with Abrupt Junctions 235 -- 20.3.3 Behaviors of Drivability and Off‐Current 237 -- 20.3.4 Dynamic Performance of Devices with Graded‐Profile Junctions 239 -- 20.4 Summary 239 -- References 240 -- Part V POTENTIAL OF PARTIALLY DEPLETED SOI MOSFETs 241 -- 21 Proposal for Cross‐Current Tetrode (XCT) SOI MOSFETs: A 60 dB Single‐Stage CMOS Amplifier Using High‐Gain Cross‐Current Tetrode MOSFET/SIMOX 243 -- 21.1 Introduction 243 -- 21.2 Device Fabrication 244 -- 21.3 Device Characteristics 245 -- 21.4 Performance of CMOS Amplifier 247 -- 21.5 Summary 249 -- References 249 -- 22 Device Model of the XCT‐SOI MOSFET and Scaling Scheme 250 -- 22.1 Introduction 250 -- 22.2 Device Structure and Assumptions for Modeling 251 -- 22.2.1 Device Structure and Features of XCT Device 251 -- 22.2.2 Basic Assumptions for Device Modeling 253 -- 22.2.3 Derivation of Model Equations 254 -- 22.3 Results and Discussion 258 -- 22.3.1 Measured Characteristics of XCT Devices 258 -- 22.4 Design Guidelines 261 -- 22.4.1 Drivability Control 261 -- 22.4.2 Scaling Issues 262 -- 22.4.3 Potentiality of Low‐Energy Operation of XCT CMOS Devices 265 -- 22.5 Summary 267 -- 22.6 Appendix: Calculation of MOSFET Channel Current 267 -- 22.7 Appendix: Basic Condition for Drivability Control 271 -- References 271 -- 23 Low‐Power Multivoltage Reference Circuit Using XCT‐SOI MOSFET 274 -- 23.1 Introduction 274 -- 23.2 Device Structure and Assumptions for Simulations 274 -- 23.2.1 Device Structure and Features 274 -- 23.2.2 Assumptions for Simulations 277 -- 23.3 Proposal for Voltage Reference Circuits and Simulation Results 278 -- 23.3.1 Two‐Reference Voltage Circuit 278 -- 23.3.2 Three‐Reference Voltage Circuit 283 -- 23.4 Summary 283 -- References 284 -- 24 Low‐Energy Operation Mechanisms for XCT‐SOI CMOS Devices: Prospects for a Sub‐20 nm Regime 285 -- 24.1 Introduction 285 -- 24.2 Device Structure and Assumptions for Modeling 286. 24.3 Circuit Simulation Results of SOI CMOS and XCT‐SOI CMOS 288 -- 24.4 Further Scaling Potential of XCT‐SOI MOSFET 291 -- 24.5 Performance Expected from the Scaled XCT‐SOI MOSFET 292 -- 24.6 Summary 296 -- References 296 -- Part VI QUANTUM EFFECTS AND APPLICATIONS / 1 297 -- 25 Overview 299 -- References 299 -- 26 Si Resonant Tunneling MOS Transistor 301 -- 26.1 Introduction 301 -- 26.2 Configuration of SRTMOST 302 -- 26.2.1 Structure and Electrostatic Potential 302 -- 26.2.2 Operation Principle and Subthreshold Characteristics 304 -- 26.3 Device Performance of SRTMOST 307 -- 26.3.1 Transistor Characteristics of SRTMOST 307 -- 26.3.2 Logic Circuit Using SRTMOST 310 -- 26.4 Summary 312 -- References 312 -- 27 Tunneling Dielectric Thin‐Film Transistor 314 -- 27.1 Introduction 314 -- 27.2 Fundamental Device Structure 315 -- 27.3 Experiment 315 -- 27.3.1 Experimental Method 315 -- 27.3.2 Calculation Method 317 -- 27.4 Results and Discussion 320 -- 27.4.1 Evaluation of SiNx Film 320 -- 27.4.2 Characteristics of the TDTFT 320 -- 27.4.3 TFT Performance at Low Temperatures 324 -- 27.4.4 TFT Performance at High Temperatures 324 -- 27.4.5 Suppression of the Hump Effect by the TDTFT 330 -- 27.5 Summary 336 -- References 336 -- 28 Proposal for a Tunnel‐Barrier Junction (TBJ) MOSFET 339 -- 28.1 Introduction 339 -- 28.2 Device Structure and Model 339 -- 28.3 Calculation Results 340 -- 28.4 Summary 343 -- References 343 -- 29 Performance Prediction of SOI Tunneling‐Barrier‐Junction MOSFET 344 -- 29.1 Introduction 344 -- 29.2 Simulation

Model 345 -- 29.3 Simulation Results and Discussion 349 -- 29.3.1 Fundamental Properties of TBJ MOSFET 349 -- 29.3.2 Optimization of Device Parameters and Materials 349 -- 29.4 Summary 357 -- References 357 -- 30 Physics-Based Model for TBJ MOSFETs and High-Frequency Performance Prospects 358 -- 30.1 Introduction 358 -- 30.2 Device Structure and Device Model for Simulations 359 -- 30.3 Simulation Results and Discussion 360 -- 30.3.1 Current Drivability 361. 30.3.2 Threshold Voltage Issue 362 -- 30.3.3 Subthreshold Characteristics 363 -- 30.3.4 Radio-Frequency Characteristics 363 -- 30.4 Summary 365 -- References 365 -- 31 Low-Power High-Temperature-Operation-Tolerant (HTOT) SOI MOSFET 367 -- 31.1 Introduction 367 -- 31.2 Device Structure and Simulations 368 -- 31.3 Results and Discussion 371 -- 31.3.1 Room-Temperature Characteristics 371 -- 31.3.2 High-Temperature Characteristics 373 -- 31.4 Summary 377 -- References 379 -- Part VII QUANTUM EFFECTS AND APPLICATIONS / 2 381 -- 32 Overview of Tunnel Field-Effect Transistor 383 -- References 385 -- 33 Impact of a Spacer Dielectric and a Gate Overlap/Underlap on the Device Performance of a Tunnel Field-Effect Transistor 386 -- 33.1 Introduction 386 -- 33.2 Device Structure and Simulation 387 -- 33.3 Results and Discussion 387 -- 33.3.1 Effects of Variation in the Spacer Dielectric Constant 387 -- 33.3.2 Effects of Variation in the Spacer Width 391 -- 33.3.3 Effects of Variation in the Source Doping Concentration 392 -- 33.3.4 Effects of a Gate-Source Overlap 394 -- 33.3.5 Effects of a Gate-Channel Underlap 394 -- 33.4 Summary 397 -- References 397 -- 34 The Impact of a Fringing Field on the Device Performance of a P-Channel Tunnel Field-Effect Transistor with a High-Gate Dielectric 399 -- 34.1 Introduction 399 -- 34.2 Device Structure and Simulation 399 -- 34.3 Results and Discussion 400 -- 34.3.1 Effects of Variation in the Gate Dielectric Constant 400 -- 34.3.2 Effects of Variation in the Spacer Dielectric Constant 408 -- 34.4 Summary 410 -- References 410 -- 35 Impact of a Spacer-Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling 412 -- 35.1 Introduction 412 -- 35.2 Device Structure and Process Steps 413 -- 35.3 Simulation Setup 414 -- 35.4 Results and Discussion 416 -- 35.4.1 Impact of Variation in the Spacer-Drain Overlap 416 -- 35.4.2 Influence of Drain on the Device Characteristics 424 -- 35.4.3 Impact of Scaling 426. 35.5 Summary 429 -- References 430 -- 36 Gate-on-Germanium Source Tunnel Field-Effect Transistor Enabling Sub-0.5V Operation 431 -- 36.1 Introduction 431 -- 36.2 Proposed Device Structure 431 -- 36.3 Simulation Setup 432 -- 36.4 Results and Discussion 434 -- 36.4.1 Device Characteristics 434 -- 36.4.2 Effects of Different Structural Parameters 435 -- 36.4.3 Optimization of Different Structural Parameters 436 -- 36.5 Summary 445 -- References 445 -- Part VIII PROSPECTS OF LOW-ENERGY DEVICE TECHNOLOGY AND APPLICATIONS 447 -- 37 Performance Comparison of Modern Devices 449 -- References 450 -- 38 Emerging Device Technology and the Future of MOSFET 452 -- 38.1 Studies to Realize High-Performance MOSFETs based on Unconventional Materials 452 -- 38.2 Challenging Studies to Realize High-Performance MOSFETs based on the Nonconventional Doctrine 453 -- References 454 -- 39 How Devices Are and Should Be Applied to Circuits 456 -- 39.1 Past Approach 456 -- 39.2 Latest Studies 456 -- References 457 -- 40 Prospects for Low-Power

