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Nota di contenuto	Chapter 1. Introduction -- Chapter 2. State of the Art -- Chapter 3. Modeling Cell-internal EM -- Chapter 4. Current Calculation -- Chapter 5. Experimental Setup -- Chapter 6.Results -- Chapter 7. Analyzing the Electromigration Effects on Different Metal Layers -- Chapter 8. Conclusions.
Sommario/riassunto	This book describes new and effective methodologies for modeling, analyzing and mitigating cell-internal signal electromigration in nanoCMOS, with significant circuit lifetime improvements and no impact on performance, area and power. The authors are the first to analyze and propose a solution for the electromigration effects inside logic cells of a circuit. They show in this book that an interconnect inside a cell can fail reducing considerably the circuit lifetime and they demonstrate a methodology to optimize the lifetime of circuits, by placing the output, Vdd and Vss pin of the cells in the less critical regions, where the electromigration effects are reduced. Readers will be enabled to apply this methodology only for the critical cells in the circuit, avoiding impact in the circuit delay, area and performance, thus

increasing the lifetime of the circuit without loss in other characteristics. .