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Note generali	Bibliographic Level Mode of Issuance: Monograph
Sommario/riassunto	This paper presents a new trace-back memory structure for Viterbi decoders that reduces power consumption by 63% compared to the conventional RAM based design. Instead of the intensive read and write operations as required in RAM based designs, the new memory is based on an array of registers connected with trace-back signals that decode the output bits on the fly. The structure is used together with appropriate clock and power-aware control signals. Based on a 0.35 /spl mu/m CMOS implementation the trace-back back memory consumes energy of 182 pJ.

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