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Sommario/riassunto	This document specifies a standard for use of very high-speed integrated circuit hardwaredescription language (VHDL) to model synthesizable register-transfer level digital logic. Astandard syntax and semantics for VHDL register-transfer level synthesis is defined. The subset ofthe VHDL language, which is synthesizable, is described, and nonsynthesizable VHDL constructsare identified that should be ignored or flagged as errors.