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Sommario/riassunto	This standard represents a merger of two previous standards: IEEE 1364-2005 Verilog hardware description language (HDL) and IEEE 1800-2005 SystemVerilog unified hardware design, specification and verification language. The 2005 SystemVerilog standard defines extensions to the 2005 Verilog standard. These two standards were designed to be used as one language. Merging the base Verilog language and the SystemVerilog extensions into a single standard enables users to have all information regarding syntax and semantics in a single document.