1. Record Nr. UNINA9910146789203321

Titolo	2005 IEEE international conference on field programmable technology
Pubbl/distr/stampa	[Place of publication not identified], : IEEE, 2005
ISBN	9781509099498 1509099492
Descrizione fisica	1 online resource (xxii, 344 pages) : illustrations
Disciplina	025.21
Soggetti	Field programmable gate arrays
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	Platform-based synthesis for field-programmable SOCs," -- Low power and high speed issues in FPGA chips," -- System architectures and design patterns for reconfigurable computing," -- Reconfigurable hardware operating systems," -- A custom instruction approach for hardware and software implementations of finite field arithmetic over F/sub 2163/ using Gaussian normal bases,"M. -- High-radix systolic modular multiplication on reconfigurable hardware," -- Pipelining saturated accumulation," -- A parameterized floating-point exponential function for FPGAs," -- The Erlangen slot machine: increasing flexibility in FPGA-based reconfigurable platforms," -- Task placement for heterogeneous reconfigurable architectures," -- A framework for dynamic resource assignment and scheduling on reconfigurable mixed-mode on-chip multiprocessors," -- High quality uniform random number generation through LUT optimised linear recurrences," -- Solving the minimum dominating set problem with instance-specific hardware on FPGAs," -- Custom hardware architectures for posture analysis," -- Correlation-based fingerprint matching using FPGAs," -- A single-chip FPGA implementation of real-time adaptive background model," -- FPGA-based hardware for physical modelling sound synthesis by finite difference schemes," -- Have GPUs made FPGAs redundant in the field of video processing?," -- S5: the architecture and development flow of a software configurable processor," -- RoMultiC: fast and simple configuration data multicasting scheme for coarse grain reconfigurable devices," --

Pipeline scheduling for array based reconfigurable architectures considering interconnect delays," -- High-speed hardware architectures of the Whirlpool hash function," -- Secure partial reconfiguration of FPGAs," -- An adaptive cryptographic accelerator for IPsec on dynamically reconfigurable processor," -- Dynamic voltage scaling for commercial FPGAs," -- FPGA defect tolerance: impact of granularity," -- A dynamically reconfigured UMTS multi-channel complex code matched filter," -- Prototyping automatic cloud cover assessment (ACCA) algorithm for remote sensing on-board processing on a reconfigurable computer,"E. -- Reconfigurable acceleration for Monte Carlo based financial simulation," -- Accelerating FPGA routing using architecture-adaptive A* techniques," -- Compiler-directed design space exploration for caching and prefetching data in high-level synthesis," -- Post-silicon debug using programmable logic cores," -- FPGA organization for the fast path-based neural branch predictor," -- FPGA implementation of an excitatory and inhibitory connectionist model for motion perception," -- Spatiotemporal simulation of a single living cell," -- Dynamic loading of peripherals on reconfigurable system-on-chip," -- An FPGA model for developing dynamic circuit computing," -- ADH: an aspect described hardware programming language," -- From TLM to FPGA: rapid prototyping with SystemC and transaction level modeling," -- Rapid reconfiguration of an optically differential reconfigurable gate array with pulse lasers," -- Hardware-accelerated SSH on self-reconfigurable systems," -- A fast and efficient FPGA-based implementation for solving a system of linear interval equations," -- Heuristics for context-caches in 2-level reconfigurable architectures," -- Performance of sorting algorithms on the SRC 6 reconfigurable computer," -- A zero-overhead dynamic optically reconfigurable gate array," -- The Transmogrifier-4: an FPGA-based hardware development system with multi-gigabyte memory capacity and high host and memory bandwidth," -- High performance channel model hardware emulator for 802.11n," -- HW/SW interface synthesis based on Avalon bus specification for Nios-oriented SoC design," -- A reconfigurable architecture for implementing multiple cipher algorithms," -- Low latency elliptic curve cryptography accelerators for NIST curves over binary fields," -- A system-level design methodology for reconfigurable computing applications," -- Optimal FFT architecture selection for OFDM receivers on FPGA," -- An FPGA-based infant monitoring system," -- FPGA-based conformance testing and system prototyping of an MPEG-4 SA-DCT hardware accelerator," -- FPGA core network implementation and optimization: a case study," -- A state-serial Viterbi decoder architecture for digital radio on FPGA," -- A design methodology to generate dynamically self-reconfigurable SoCs for Virtex-II Pro FPGAs," -- Implementation of Gabor-type filters on field programmable gate arrays,"O. -- A scaleable FFT/IFFT kernel for communication systems using codesign approach," -- FPGA based router for cognitive packet networks," -- An overview of high-level synthesis of multiprocessors for logic programming," -- Implementation of EAX mode of operation for FPGA bitstream encryption and authentication," -- Net power directed clustering algorithm for low net-power implementation of FPGAs," -- The design of scalable stochastic biochemical simulator on FPGA," -- Designing an FPGA SoC using a standardized IP block interface,".

Sommario/riassunto

Aggressive pipelining allows FPGAs to achieve high throughput on many Digital Signal Processing applications. However, cyclic data dependencies in the computation can limit pipelining and reduce the efficiency and speed of an FPGA implementation. Saturated accumulation is an important example where such a cycle limits the

throughput of signal processing applications. We show how to reformulate saturated addition as an associative operation so that we can use a parallel-prefix calculation to perform saturated accumulation at any data rate supported by the device. This allows us, for example, to design a 16-bit saturated accumulator which can operate at 280MHz on a Xilinx Spartan-3 (XC3S-5000-4), the maximum frequency supported by the component's DCM.