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Nota di contenuto	NANO-CMOS CIRCUIT AND PHYSICAL DESIGN; CONTENTS; FOREWORD; PREFACE; 1 NANO-CMOS SCALING PROBLEMS AND IMPLICATIONS; 1.1 Design Methodology in the Nano-CMOS Era; 1.2 Innovations Needed to Continue Performance Scaling; 1.3 Overview of Sub-100-nm Scaling Challenges and Subwavelength Optical Lithography; 1.3.1 Back-End-of-Line Challenges (Metallization); 1.3.2 Front-End-of-Line Challenges (Transistors); 1.4 Process Control and Reliability; 1.5 Lithographic Issues and Mask Data Explosion; 1.6 New Breed of Circuit and Physical Design Engineers; 1.7 Modeling Challenges 1.8 Need for Design Methodology Changes1.9 Summary; References; PART I PROCESS TECHNOLOGY AND SUBWAVELENGTH OPTICAL LITHOGRAPHY: PHYSICS, THEORY OF OPERATION, ISSUES, AND SOLUTIONS; 2 CMOS DEVICE AND PROCESS TECHNOLOGY; 2.1 Equipment Requirements for Front-End Processing; 2.1.1 Technical Background; 2.1.2 Gate Dielectric Scaling; 2.1.3 Strain Engineering; 2.1.4 Rapid Thermal Processing Technology; 2.2 Front-End-Device Problems in CMOS Scaling; 2.2.1 CMOS Scaling Challenges; 2.2.2

Quantum Effects Model; 2.2.3 Polysilicon Gate Depletion Effects; 2.2.4 Metal Gate Electrodes
2.2.5 Direct-Tunneling Gate Leakage2.2.6 Parasitic Capacitance; 2.2.7 Reliability Concerns; 2.3 Back-End-of-Line Technology; 2.3.1 Interconnect Scaling; 2.3.2 Copper Wire Technology; 2.3.3 Low-Dielectric Challenges; 2.3.4 Future Global Interconnect Technology; References; 3 THEORY AND PRACTICALITIES OF SUBWAVELENGTH OPTICAL LITHOGRAPHY; 3.1 Introduction and Simple Imaging Theory; 3.2 Challenges for the 100-nm Node; 3.2.1 -Factor for the 100-nm Node; 3.2.2 Significant Process Variations; 3.2.3 Impact of Low- Imaging on Process Sensitivities; 3.2.4 Low- Imaging and Impact on Depth of Focus
3.2.5 Low- Imaging and Exposure Tolerance3.2.6 Low- Imaging and Impact on Mask Error Enhancement Factor; 3.2.7 Low- Imaging and Sensitivity to Aberrations; 3.2.8 Low- Imaging and CD Variation as a Function of Pitch; 3.2.9 Low- Imaging and Corner Rounding Radius; 3.3 Resolution Enhancement Techniques: Physics; 3.3.1 Specialized Illumination Patterns; 3.3.2 Optical Proximity Corrections; 3.3.3 Subresolution Assist Features; 3.3.4 Alternating Phase-Shift Masks; 3.4 Physical Design Style Impact on RET and OPC Complexity; 3.4.1 Specialized Illumination Conditions
3.4.2 Two-Dimensional Layouts3.4.3 Alternating Phase-Shift Masks; 3.4.4 Mask Costs; 3.5 The Road Ahead: Future Lithographic Technologies; 3.5.1 The Evolutionary Path: 157-nm Lithography; 3.5.2 Still Evolutionary: Immersion Lithography; 3.5.3 Quantum Leap: EUV Lithography; 3.5.4 Particle Beam Lithography; 3.5.5 Direct-Write Electron Beam Tools; References; PART II PROCESS SCALING IMPACT ON DESIGN; 4 MIXED-SIGNAL CIRCUIT DESIGN; 4.1 Introduction; 4.2 Design Considerations; 4.3 Device Modeling; 4.4 Passive Components; 4.5 Design Methodology; 4.5.1 Benchmark Circuits
4.5.2 Design Using Thin Oxide Devices

Sommario/riassunto

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.