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Nota di contenuto	DEDICATED DIGITAL PROCESSORS; Contents; Preface; 1 Digital Computer Basics; 1.1 Data Encoding; 1.1.1 Encoding Numbers; 1.1.2 Code Conversions and More Codes; 1.2 Algorithms and Algorithmic Notations; 1.2.1 Functional Composition and the Data Flow; 1.2.2 Composition by Cases and the Control Flow; 1.2.3 Alternative Algorithms; 1.3 Boolean Functions; 1.3.1 Sets of Elementary Boolean Operations; 1.3.2 Gate Complexity and Simplification of Boolean Algorithms; 1.3.3 Combined and Universal Functions; 1.4 Timing, Synchronization and Memory; 1.4.1 Processing Time and Throughput of Composite Circuits 1.4.2 Serial and Parallel Processing 1.4.3 Synchronization; 1.5 Aspects of System Design; 1.5.1 Architectures for Digital Systems; 1.5.2 Application Modeling; 1.5.3 Design Metrics; 1.6 Summary; Exercises; 2 Hardware Elements; 2.1 Transistors, Gates and Flip-Flops; 2.1.1 Implementing Gates with Switches; 2.1.2 Registers and Synchronization Signals; 2.1.3 Power Consumption and Related Design Rules; 2.1.4 Pulse Generation and Interfacing; 2.2 Chip Technology; 2.2.1 Memory

Bus Interface; 2.2.2 Semiconductor Memory Devices; 2.2.3 Processors and Single-Chip Systems; 2.2.4 Configurable Logic, FPGA  
2.3 Chip Level and Circuit Board-Level Design2.3.1 Chip Versus Board-Level Design; 2.3.2 IP-Based Design; 2.3.3 Configurable Boards and Interconnections; 2.3.4 Testing; 2.4 Summary; Exercises; 3 Hardware Design Using VHDL; 3.1 Hardware Design Languages; 3.2 Entities and Signals; 3.3 Functional Behavior of Building Blocks; 3.4 Structural Architecture Definitions; 3.5 Timing Behavior and Simulation; 3.6 Test Benches; 3.7 Synthesis Aspects; 3.8 Summary; Exercises; 4 Operations on Numbers; 4.1 Single Bit Binary Adders and Multipliers; 4.2 Fixed Point Add, Subtract, and Compare  
4.3 Add and Subtract for Redundant Codes4.4 Binary Multiplication; 4.5 Sequential Adders, Multipliers and Multiply-Add Structures; 4.6 Distributed Arithmetic; 4.7 Division and Square Root; 4.8 Floating Point Operations and Functions; 4.9 Polynomial Arithmetic; 4.10 Summary; Exercises; 5 Sequential Control Circuits; 5.1 Mealy and Moore Automata; 5.2 Scheduling, Operand Selection and the Storage Automaton; 5.3 Designing the Control Automaton; 5.4 Sequencing with Counter and Shift Register Circuits; 5.5 Implementing the Control Flow; 5.6 Synchronization; 5.7 Summary; Exercises  
6 Sequential Processors6.1 Designing for ALU Efficiency; 6.1.1 Multifunction ALU Circuits; 6.1.2 Pipelining; 6.2 The Memory Subsystem; 6.2.1 Pipelined Memory Accesses, Registers, and the Von Neumann Architecture; 6.2.2 Instruction Set Architectures and Memory Requirements; 6.2.3 Caches and Virtual Memory, Soft Caching; 6.3 Simple Programmable Processor Designs; 6.3.1 CPU1 - The Basic Control Function; 6.3.2 CPU2 - An Efficient Processor for FPGA-based Systems; 6.4 Interrupt Processing and Context Switching; 6.5 Interfacing Techniques; 6.5.1 Pipelining Input and Output  
6.5.2 Parallel and Serial Interfaces, Counters and Timers

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#### Sommario/riassunto

The recent evolution of digital technology has resulted in the design of digital processors with increasingly complex capabilities. The implementation of hardware/software co-design methodologies provides new opportunities for the development of low power, high speed DSPs and processor networks. Dedicated digital processors are digital processors with an application specific computational task. Dedicated Digital Processors presents an integrated and accessible approach to digital processor design principles, processes, and implementations based upon the author's considerable experience

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