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Titolo	Evaluating the impact of leadership development / / Tracy E. Patterson [and four others]
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ISBN	1-60491-647-8
Edizione	[Second edition.]
Descrizione fisica	1 online resource (121 pages)
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Soggetti	Leadership - Evaluation Executives - Training of - Evaluation Electronic books.
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Nota di bibliografia	Includes bibliographical references.
Sommario/riassunto	Driving impact while managing resources are what most organizations strive to balance in their leadership-development efforts. Evaluation provides a practical framework for gathering and making sense of information to better manage resources while assessing the success of leadership-development efforts. This second edition of Evaluating the Impact of Leadership Development is a practical guide for human-resource professionals, consultants, managers, employees, and volunteers who have leadership-development or evaluation responsibilities in their organizations and want to enhance their practice and demonstrate the value of their work.

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Autore	Kinniment D. J (David John)
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Nota di contenuto	Synchronization and Arbitration in Digital Systems; Contents; Preface; List of Contributors; Acknowledgements; 1 Synchronization, Arbitration and Choice; 1.1 INTRODUCTION; 1.2 THE PROBLEM OF CHOICE; 1.3 CHOICE IN ELECTRONICS; 1.4 ARBITRATION; 1.5 CONTINUOUS AND DISCRETE QUANTITIES; 1.6 TIMING; 1.7 BOOK STRUCTURE; Part I; 2 Modelling Metastability; 2.1 THE SYNCHRONIZER; 2.2 LATCH MODEL; 2.3 FAILURE RATES; 2.3.1 Event Histograms and MTBF; 2.4 LATCHES AND FLIP-FLOPS; 2.5 CLOCK BACK EDGE; 3 Circuits; 3.1 LATCHES AND METASTABILITY FILTERS; 3.2 EFFECTS OF FILTERING; 3.3 THE JAMB LATCH 3.3.1 Jamb Latch Flip-. op3.4 LOW COUPLING LATCH; 3.5 THE Q-FLOP; 3.6 THE MUTEX; 3.7 ROBUST SYNCHRONIZER; 3.8 THE TRI-FLOP; 4 Noise and its Effects; 4.1 NOISE; 4.2 EFFECT OF NOISE ON A SYNCHRONIZER; 4.3 MALICIOUS INPUTS; 4.3.1 Synchronous Systems; 4.3.2 Asynchronous Systems; 5 Metastability Measurements; 5.1 CIRCUIT SIMULATION; 5.1.1 Time Step Control; 5.1.2 Long-term ; 5.1.3 Using Bisection; 5.2 SYNCHRONIZER FLIP-FLOP TESTING; 5.3 RISING AND FALLING EDGES; 5.4 DELAY-BASED MEASUREMENT; 5.5

DEEP METASTABILITY; 5.6 BACK EDGE MEASUREMENT; 5.7 MEASURE AND SELECT; 5.7.1 Failure Measurement
5.7.2 Synchronizer Selection6 Conclusions Part I; Part II; 7 Synchronizers in Systems; 7.1 LATENCY AND THROUGHPUT; 7.2 FIFO SYNCHRONIZER; 7.3 AVOIDING SYNCHRONIZATION; 7.4 PREDICTIVE SYNCHRONIZERS; 7.5 OTHER LOW-LATENCY SYNCHRONIZERS; 7.5.1 Locally Delayed Latching (LDL); 7.5.2 Speculative Synchronization; 7.5.2.1 Synchronization error detection; 7.5.2.2 Pipelining; 7.5.2.3 Recovery; 7.6 ASYNCHRONOUS COMMUNICATION MECHANISMS (ACM); 7.6.1 Slot Mechanisms; 7.6.2 Three-slot Mechanism; 7.6.3 Four-slot Mechanism; 7.6.4 Hardware Design and Metastability; 7.7 SOME COMMON SYNCHRONIZER DESIGN ISSUES
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12.1.1 Two-phase or Non-return-to-zero (NRZ) Protocols

Sommario/riassunto

Today's networks of processors on and off chip, operating with independent clocks, need effective synchronization of the data passing between them for reliability. When two or more processors request access to a common resource, such as a memory, an arbiter has to decide which request to deal with first. Current developments in integrated circuit processing are leading to an increase in the numbers of independent digital processing elements in a single system. With this comes faster communications, more networks on chip, and the demand for more reliable, more complex, and higher performance sy

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