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Nota di contenuto	Proceedings. 24th IEEE VLSI Test Symposium -- 24th IEEE VLSI Test Symposium - Title -- 24th IEEE VLSI Test Symposium - Copyright -- 24th IEEE Symposium on Reliable Distributed Systems - Table of contents -- Forward -- Organizing Committee -- Program Committee -- Reviewers -- Acknowledgments -- Test Technology Technical Council (TTTC) -- Awards -- Test Technology Educational Program (TTEP) Tutorials -- The impacts of untestable defects on transition fault testing -- Low-cost scan-based delay testing of latch-based circuits with time borrowing -- Path delay fault simulation on large industrial designs -- A scheme for on-chip timing characterization -- BIST for network-on-chip interconnect infrastructures.
Sommario/riassunto	Annotation VTS 2006 focuses on innovation in the field of testing of integrated circuits and systems. VTS looks at the many trends and challenges in the semiconductor design and manufacturing industries with papers covering wide range of interests, including basic and continuing education for test professionals, the latest research developments, new directions and hot topics in test, and expert perspectives on current issues. The proceedings explores high speed interconnect testing, analog and mixed signal testing, delay testing, flash and memory testing, RF testing, yield analysis, nanoscale testing, IDDQ, MEMS, and wireless testing.

