

1. Record Nr.	UNINA9910144576103321
Autore	Goel Ashok K. <1953->
Titolo	High-speed VLSI interconnections // Ashok K. Goel
Pubbl/distr/stampa	Hoboken, N.J., : Wiley-Interscience, : IEEE Press, c2007
ISBN	1-281-09414-5 9786611094140 0-470-16597-9 0-470-16596-0
Edizione	[2nd ed.]
Descrizione fisica	1 online resource (433 p.)
Collana	Wiley series in microwave and optical engineering
Disciplina	621.39/5
Soggetti	Very high speed integrated circuits - Mathematical models Very high speed integrated circuits - Defects - Mathematical models Integrated circuits - Very large scale integration - Computer simulation Semiconductors - Junctions
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Description based upon print version of record.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Preface -- 1. Preliminary Concepts and More -- 1.1 Interconnections for VLSI Applications -- 1.1.1 Metallic Interconnections - Multilevel, Multilayer and Multipath Configurations -- 1.1.2 Optical Interconnections -- 1.1.3 Superconducting Interconnections -- 1.2 Copper Interconnections -- 1.2.1 Advantages of Copper Interconnections -- 1.2.2 Challenges Posed by Copper Interconnections -- 1.2.3 Fabrication Processes for Copper Interconnections -- 1.2.4 Damascene Processing of Copper Interconnections -- 1.3 Method of Images -- 1.4 Method of Moments -- 1.5 Even and Odd Mode Capacitances -- 1.5.1 Two Coupled Conductors -- 1.5.2 Three Coupled Conductors -- 1.6 Transmission Line Equations -- 1.7 Miller's Theorem -- 1.8 Inverse Laplace Transformation -- 1.9 A Resistive Interconnection as a Ladder Network -- 1.9.1 Open Circuit Interconnection -- 1.9.2 Short Circuited Interconnection -- 1.9.3 Application of the Ladder Approximation to a Multipath Interconnection -- 1.10 Propagation Modes in a Microstrip Interconnection -- 1.11 Slow-Wave Mode Propagation -- 1.11.1 Quasi-TEM Analysis -- 1.11.2 Comparison with Experimental Results -- 1.12 Propagation Delays --

Exercises -- References -- 2. Parasitic Resistances, Capacitances and Inductances -- 2.1 Parasitic Resistances - General Considerations -- 2.2 Parasitic Capacitances - General Considerations -- 2.2.1 Parallel Plate Capacitance -- 2.2.2 Fringing Capacitances -- 2.2.3 Coupling Capacitances -- 2.3 Parasitic Inductances - General Considerations -- 2.3.1 Self and Mutual Inductances -- 2.3.2 Partial Inductances -- 2.3.3 Methods for Inductance Extraction -- 2.3.4 Effect of Inductances on Interconnection Delays -- 2.4 Approximate Formulas for Capacitances -- 2.4.1 Single Line on a Ground Plane -- 2.4.2 Two Lines on a Ground Plane -- 2.4.3 Three Lines on a Ground Plane -- 2.4.4 Single Plate with Finite Dimensions on a Ground Plane -- 2.5 The Green's Function Method - Using Method of Images. 2.5.1 Green's Function Matrix for Interconnections Printed on the Substrate -- 2.5.2 Green's Function Matrix for Interconnections Embedded in the Substrate -- 2.5.3 Application of the Method of Moments -- 2.5.4 Even and Odd Mode Capacitances -- 2.5.5 Ground and Coupling Capacitances -- 2.5.6 The Program IPCSGV -- 2.5.7 Parametric Dependence of Interconnection Capacitances -- 2.6 The Green's Function Method - Fourier Integral Approach -- 2.6.1 Green's Function for Multilevel Interconnections -- 2.6.2 Multiconductor Interconnection Capacitances -- 2.6.3 Piecewise Linear Charge Distribution Function -- 2.6.4 Calculation of Interconnection Capacitances -- 2.7 The Network Analogue Method -- 2.7.1 Representation of Subregions by Network Analogues -- 2.7.2 Diagonalized System for Single Level Interconnections -- 2.7.3 Diagonalized System for Multilevel Interconnections -- 2.7.4 Interconnection Capacitances and Inductances -- 2.7.5 The Program "ICIMPGV" -- 2.7.6 Parametric Dependence of Interconnection Capacitances -- 2.7.7 Parametric Dependence of Interconnection Inductances -- 2.8 Simplified Formulas for Interconnection Capacitances and Inductances on Silicon and GaAs Substrates -- 2.8.1 Line Capacitances and Inductances -- 2.8.2 Coupling Capacitances and Inductances -- 2.9 Inductance Extraction Using FastHenry -- 2.9.1 The Program "FastHenry" -- 2.9.2 Extraction Results Using FastHenry -- 2.10 Copper Interconnections - Resistance Modeling -- 2.10.1 Effect of Surface/Interface Scattering on the Interconnection Resistivity -- 2.10.2 Effect of Diffusion Barrier on the Interconnection Resistivity -- 2.11 Electrode Capacitances in a GaAs MESFET - An Application of the Program IPCSGV -- 2.11.1 Ground and Coupling Capacitances -- 2.11.2 The Program "EPCSGM" -- 2.11.3 Dependence on MESFET Dimensions -- 2.11.4 Comparison with Internal MESFET Capacitances -- Exercises -- References -- 3. Interconnection Delays -- 3.1 Metal-Insulator-Semiconductor Microstrip Line Model of an Interconnection. 3.1.1 The Model -- 3.1.2 Simulation Results -- 3.2 Transmission Line Analysis of Single Level Interconnections -- 3.2.1 The Model -- 3.2.2 The Program "PDSIGV" -- 3.2.3 Dependence on Interconnection Parameters -- 3.3 Transmission Line Analysis of Parallel Multilevel Interconnections -- 3.3.1 The Model -- 3.3.2 Numerical Simulation Results -- 3.4 Analysis of Crossing Interconnections -- 3.4.1 Simplified Analysis of Crossing Interconnections -- 3.4.2 Comprehensive Analysis of Crossing Interconnections -- 3.4.3 The Program "SPBIGV" -- 3.4.4 Simulation Results Using SPBIGV 3.5 Parallel Interconnections Modeled as Multiple Coupled Microstrips -- 3.5.1 The Model -- 3.5.2 Simulation Results -- 3.6 Modeling of Lossy Parallel and Crossing Interconnections as Coupled Lumped Distributed Systems -- 3.6.1 The Model -- 3.6.2 Simulation Results -- 3.7 Very High Frequency Losses in a Microstrip

Interconnection -- 3.7.1 The Model -- 3.7.2 Simulation Results --
3.7.3 Interconnection Delays With the High-Frequency Effects -- 3.8
Compact Expressions for Interconnection Delays -- 3.8.1 The RC
Interconnection Model -- 3.8.2 The RLC Interconnection Model - A
Single Semi-Infinite Line -- 3.8.3 The RLC Interconnection Model - A
Single Finite Line -- 3.8.4 Single RLC Interconnection - Delay Time --
3.8.5 Two and Three Coupled RLC Interconnections - Delay Times --
3.9 Interconnection Delays in Multilayer Integrated Circuits -- 3.9.1
The Simplified Model -- 3.9.2 Simulation Results and Discussion --
3.10 Active Interconnections -- 3.10.1 Interconnection Delay Model --
3.10.2 Active Interconnection Driven by Minimum Size Inverters --
3.10.3 Active Interconnection Driven by Optimum Size Inverters --
3.10.4 Active Interconnection Driven by Cascaded Inverters -- 3.10.5
Dependence of Propagation Time on the Interconnection Driving
Mechanism -- Exercises -- References -- 4. Crosstalk Analysis -- 4.1
Lumped Capacitance Approximation -- 4.2 Coupled Multiconductor MIS
Microstrip Line Model of Single Level Interconnections.
4.2.1 The Model -- 4.2.2 Numerical Simulations -- 4.2.3 Crosstalk
Reduction -- 4.3 Frequency Domain Modal Analysis of Single Level
Interconnections -- 4.3.1 The General Technique -- 4.3.2 Two-Line
System -- 4.3.3 Three-Line System -- 4.3.4 Four-Line System -- 4.3.5
Simulation Results -- 4.4 Transmission Line Analysis of Parallel
Multilevel Interconnections -- 4.4.1 The Model -- 4.4.2 The Program
"DCMPVI" -- 4.4.3 Numerical Simulations Using DCMPVI --
4.5 Analysis of Crossing Interconnections -- 4.5.1 Effect of Crossing
Interconnections -- 4.5.2 Comprehensive Analysis of Crossing
Interconnections -- 4.6 Compact Expressions for Crosstalk Analysis --
4.6.1 Distributed RC Model for Two Coupled Interconnections -- 4.6.2
Distributed RLC Model for Two Coupled Interconnections -- 4.6.3
Distributed RLC Model for Three Coupled Interconnections -- 4.7
Multiconductor Buses in GaAs High-Speed Logic Circuits -- 4.7.1 The
Model -- 4.7.2 Lossless MBUS with Cyclic Boundary Conditions -- 4.7.3
Simulation Results -- Exercises -- References -- 5. Electromigration-
Induced Failure Analysis -- 5.1 Electromigration in VLSI Interconnection
Metallizations - An Overview -- 5.1.1 Problems Caused by
Electromigration -- 5.1.2 Electromigration Mechanism and Factors --
5.1.3 Electromigration Under Pulsed-DC and AC Conditions -- 5.1.4
Testing and Monitoring of Electromigration -- 5.1.5 General Guidelines
for Testing Electromigration -- 5.1.6 Reduction of Electromigration --
5.2 Models of IC Reliability -- 5.2.1 Arrhenius Model -- 5.2.2 Mil-
Hdbk-217D Model -- 5.2.3 Series Model -- 5.2.4 Series-Parallel Model
-- 5.3 Modeling of Electromigration Due to Repetitive Pulsed Currents
-- 5.3.1 Modeling of Physical Processes -- 5.3.2 First-Order Model
Development -- 5.3.3 Modeling Results for DC Currents -- 5.3.4
Modeling Results for Pulsed Currents -- 5.4 Electromigration in the
Copper Interconnections -- 5.4.1 Electromigration Under DC
Conditions -- 5.4.2 Electromigration Under Pulsed DC Condition.
5.4.3 Electromigration Under Bipolar AC Conditions -- 5.5 Failure
Analysis of VLSI Interconnection Components -- 5.5.1 Reduction of
Components into Straight Segments -- 5.5.2 Calculation of MTF and
Lognormal Standard Deviation -- 5.5.3 The Program "EMVIC"
-- 5.5.4 Simulation Results Using EMVIC -- 5.6 Computer-Aided
Failure Analysis -- 5.6.1 "RELIANT" for Reliability of VLSI
Interconnections -- 5.6.2 "SPIDER" for Checking Current
Density and Voltage Drops in the Interconnection Metallizations --
Exercises -- References -- 6. Future Interconnections -- 6.1 Optical
Interconnections -- 6.1.1 Advantages of Optical Interconnections --
6.1.2 Systems Issues and Challenges -- 6.1.3 Material Processing

Issues and Challenges -- 6.1.4 Design Issues and Challenges -- 6.2
 Transmission Line Models of Lossy Waveguide Interconnections --
 6.2.1 Lossy Waveguide with Single Propagating Wave -- 6.2.2
 Equivalent Circuits for Waveguide Drivers and Loads -- 6.2.3 Lossy
 Waveguide in an Inhomogeneous Medium -- 6.3 Superconducting
 Interconnections -- 6.3.1 Advantages of Superconducting
 Interconnections -- 6.3.2 Propagation Characteristics of
 Superconducting Interconnections -- 6.3.3 Comparison with Normal
 Metal Interconnections -- 6.4 Nanotechnology Circuit Interconnections
 - Potential Technologies -- 6.4.1 Silicon Nanowires and Metallic
 Interconnections -- 6.4.2 Nanotube Interconnections -- 6.4.3 Quantum
 Cell Based Wireless Interconnections -- 6.5 Nanotube Integrated
 Circuits -- 6.5.1 Nanotube Interconnections and Vias -- 6.5.2
 Comparison of Nanotube and Copper Interconnections -- 6.5.3
 Nanotubes for High Frequency Applications -- Exercises -- References
 -- CD-ROM -- Appendix 2.1: Listing of the Program
 "IPCSGV" for Calculating the Parasitic Capacitances for Single
 Level Interconnections on GaAs-Based VLSI Using the Green's Function
 Method -- Appendix 2.2: Listing of the Program "ICIMPGV"
 for Calculating the Parasitic Capacitances and Inductances for Multilevel
 Interconnections on GaAs-Based VLSI Using the Network Analogue
 Method.
 Appendix 2.3: Listing of the Program "EPCSGM" for
 Calculating the Electrode Parasitic Capacitances in a Single-Gate GaAs
 MESFET -- Appendix 3.1: Listing of the Program "PDSIGV" for
 Calculating the Propagation Delays in the Single Level Interconnections
 on GaAs-Based VLSI -- Appendix 3.2: Listing of the Program "IPDMSR"
 for Calculating the Propagation delays in an Interconnection Driven by
 Minimum Size Repeaters -- Appendix 3.3: Listing of the Program
 "IPDOSR" for Calculating the Propagation delays in an Interconnection
 Driven by Optimum Size Repeaters -- Appendix 3.4: Listing of the
 Program "IPDCR" for Calculating the Propagation delays in an
 Interconnection Driven by Cascaded Repeaters -- Appendix 4.1: Listing
 of the Program "DCMPVI" for Delay and Crosstalk Analysis of
 Multilevel Parallel VLSI Interconnections -- Appendix 4.2: Listing of the
 Program "SPBIGV" for Signal Propagation Analysis of Bilevel
 Crossing Interconnections on GaAs-Based VLSI -- Appendix 5.1: Listing
 of the Program "EMVIC" for Electromigration-Induced Failure
 Analysis of VLSI Interconnection Components -- Index.

Sommario/riassunto

This Second Edition focuses on emerging topics and advances in the
 field of VLSI interconnections. In the decade since High-Speed VLSI
 Interconnections was first published, several major developments have
 taken place in the field. Now, updated to reflect these advancements,
 this Second Edition includes new information on copper
 interconnections, nanotechnology circuit interconnects,
 electromigration in the copper interconnections, parasitic inductances,
 and RLC models for comprehensive analysis of interconnection delays
 and crosstalk. Each chapter is designed to exist independently or as a
 part of one coherent unit, and several appropriate exercises are
 provided at the end of each chapter, challenging the reader to gain
 further insight into the contents being discussed. Chapter subjects
 include: * Preliminary Concepts * Parasitic Resistances, Capacitances,
 and Inductances * Interconnection Delays * Crosstalk Analysis *
 Electromigration-Induced Failure Analysis * Future Interconnections
 High-Speed VLSI Interconnections, Second Edition is an indispensable
 reference for high-speed VLSI designers, RF circuit designers, and
 advanced students of electrical engineering.
