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Nota di contenuto	FSM-based Digital Design using Verilog HDL; Contents; Preface; Acknowledgements; 1 Introduction to Finite-State Machines and State Diagrams for the Design of Electronic Circuits and Systems; 1.1 INTRODUCTION; 1.2 LEARNING MATERIAL; 1.3 SUMMARY; 2 Using State Diagrams to Control External Hardware Subsystems; 2.1 INTRODUCTION; 2.2 LEARNING MATERIAL; 2.3 SUMMARY; 3 Synthesizing Hardware from a State Diagram; 3.1 INTRODUCTION TO FINITE-STATE MACHINE SYNTHESIS; 3.2 LEARNING MATERIAL; 3.3 SUMMARY; 4 Synchronous Finite-State Machine Designs; 4.1 TRADITIONAL STATE DIAGRAM SYNTHESIS METHOD 4.2 DEALING WITH UNUSED STATES4.3 DEVELOPMENT OF A HIGH/LOW ALARM INDICATOR SYSTEM; 4.3.1 Testing the Finite-State Machine using a Test-Bench Module; 4.4 SIMPLE WAVEFORM GENERATOR; 4.4.1 Sampling Frequency and Samples per Waveform; 4.5 THE DICE GAME; 4.5.1 Development of the Equations for the Dice Game; 4.6 BINARY DATA SERIAL TRANSMITTER; 4.6.1 The RE Counter Block in the Shift Register of Figure 4.15; 4.7 DEVELOPMENT OF A SERIAL ASYNCHRONOUS RECEIVER; 4.7.1 Finite-State Machine Equations; 4.8

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### Sommario/riassunto

As digital circuit elements decrease in physical size, resulting in increasingly complex systems, a basic logic model that can be used in the control and design of a range of semiconductor devices is vital. Finite State Machines (FSM) have numerous advantages; they can be applied to many areas (including motor control, and signal and serial data identification to name a few) and they use less logic than their alternatives, leading to the development of faster digital hardware systems. This clear and logical book presents a range of novel techniques for the rapid and reliable design of digit

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