Record Nr. UNINA9910144348803321 Integrated Circuit and System Design [[electronic resource]]: Power **Titolo** and Timing Modeling, Optimization and Simulation; 14th International Workshop, PATMOS 2004, Santorini, Greece, September 15-17, 2004, Proceedings / / edited by Enrico Macii, Vassilis Paliouras, Odysseas Koufopavlou Berlin, Heidelberg:,: Springer Berlin Heidelberg:,: Imprint: Springer, Pubbl/distr/stampa , 2004 3-540-30205-0 **ISBN** Edizione [1st ed. 2004.] Descrizione fisica 1 online resource (XVI, 916 p.) Lecture Notes in Computer Science, , 0302-9743 ; ; 3254 Collana Disciplina 621.3815 Soggetti **Electronics** Microelectronics Computers Logic design Computer software—Reusability Microprocessors Arithmetic and logic units, Computer Electronics and Microelectronics, Instrumentation Theory of Computation Logic Design Performance and Reliability **Processor Architectures** Arithmetic and Logic Structures Lingua di pubblicazione Inglese **Formato** Materiale a stampa Livello bibliografico Monografia Note generali Bibliographic Level Mode of Issuance: Monograph Includes bibliographical references at the end of each chapters and Nota di bibliografia index. Nota di contenuto Keynote Speech -- Invited Talks -- Embedded Tutorials -- Session 1: Buses and Communication -- Session 2: Circuits and Devices (I) --Session 3: Low Power (I) -- Session 4: Architectures -- Session 5: Asynchronous Circuits -- Session 6: System Design -- Session 7:

Circuits and Devices (II) -- Session 8: Interconnect and Physical Design

Sommario/riassunto

-- Session 9: Security and Safety -- Session 10: Low Power (II) -- Session 11: Low-Power Processing (Poster) -- Session 12: Digital Design (Poster) -- Session 13: Modeling and Simulation (Poster).

WelcometotheproceedingsofPATMOS2004,thefourteenthinaseriesofintnational workshops. PATMOS 2004 was organized by the University of Patras with technical co-sponsorship from the IEEE Circuits and Systems Society. Over the years, the PATMOS meeting has evolved into an important - ropean event, where industry and academia meet to discuss power and timing aspects in modern integrated circuit and system design. PATMOS provides a forum for researchers to discuss and investigate the emerging challenges in - sign methodologies and tools required to develop the upcoming generations of integrated circuits and systems. We realized this vision this year by providing a technical program that contained state-of-the-art technical contributions, a keynote speech, three invited talks and two embedded tutorials. The technical program focused on timing, performance and power consumption, as well as architectural aspects, with particular emphasis on modelling, design, charac- rization, analysis and optimization in the nanometer era. This year a record 152 contributions were received to be considered for p- sible presentation at PATMOS. Despite the choice for an intense three-day m- ting, only 51 lecture papers and 34 poster papers could be accommodated in the single-track technical program. The Technical Program Committee. with the - sistance of additional expert reviewers, selected the 85 papers to be presented at PATMOS and organized them into 13 technical sessions. As was the case with the PATMOS workshops, the review process was anonymous, full papers were required, and several reviews were received per manuscript.