1.	Record Nr.	UNINA9910144338003321
	Titolo	Formal Methods in Computer-Aided Design : 5th International Conference, FMCAD 2004, Austin, Texas, USA, November 15-17, 2004, Proceedings / / edited by Alan J. Hu, Andrew K. Martin
	Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 2004
	ISBN	3-540-30494-0
	Edizione	[1st ed. 2004.]
	Descrizione fisica	1 online resource (XII, 448 p.)
	Collana	Lecture Notes in Computer Science, , 0302-9743 ; ; 3312
	Disciplina	621.39/5
	Soggetti	Computer-aided engineering
		Computer hardware
		Software engineering
		Computer logic
		Logic, Symbolic and mathematical
		Artificial intelligence
		Computer-Aided Engineering (CAD, CAE) and Design
		Computer Hardware
		Software Engineering
		Logics and Meanings of Programs
		Mathematical Logic and Formal Languages
		Artificial Intelligence
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia
	Note generali	Bibliographic Level Mode of Issuance: Monograph
	Nota di bibliografia	Includes bibliographical references at the end of each chapters and index.
	Nota di contenuto	Challenges in System-Level Design -- Generating Fast Multipliers Using Clever Circuits -- Verification of Analog and Mixed-Signal Circuits Using Hybrid System Techniques -- A Methodology for the Formal Verification of FFT Algorithms in HOL -- A Functional Approach to the Formal Specification of Networks on Chip -- Proof Styles in Operational Semantics -- Integrating Reasoning About Ordinal Arithmetic into ACL2 -- Combining Equivalence Verification and Completion Functions -- Synchronization-at-Retirement for Pipeline Verification -- Late Design Changes (ECOs) for Sequentially Optimized Esterel Designs -- Non-

miter-based Combinational Equivalence Checking by Comparing BDDs with Different Variable Orders -- Scalable Automated Verification via Expert-System Guided Transformations -- Simple Yet Efficient Improvements of SAT Based Bounded Model Checking -- Simple Bounded LTL Model Checking -- QuBE++: An Efficient QBF Solver -- Bounded Probabilistic Model Checking with the Mur? Verifier -- Increasing the Robustness of Bounded Model Checking by Computing Lower Bounds on the Reachable States -- Bounded Verification of Past LTL -- A Hybrid of Counterexample-Based and Proof-Based Abstraction -- Memory Efficient All-Solutions SAT Solver and Its Application for Reachability Analysis -- Approximate Symbolic Model Checking for Incomplete Designs -- Extending Extended Vacuity -- Parameterized Vacuity -- An Operational Semantics for Weak PSL -- Accepting Predecessors Are Better than Back Edges in Distributed LTL Model-Checking -- Bloom Filters in Probabilistic Verification -- A Simple Method for Parameterized Verification of Cache Coherence Protocols -- A Partitioning Methodology for BDD-Based Verification -- Invariant Checking Combining Forward and Backward Traversal -- Variable Reuse for Efficient Image Computation.

Sommario/riassunto	These are the proceedings of the fifth international conference, Formal Methods in Computer-Aided Design (FMCAD), held 15–17 November 2004 in Austin, Texas, USA. The conference provides a forum for presenting state-of-the-art tools, methods, algorithms, and theory for the application of formalized reasoning to all aspects of computer-aided system design, including specification, verification, synthesis, and testing. FMCAD's heritage dates back 20 years to some of the earliest conferences on the subject of formal reasoning and computer-aided design. Since 1996,FMCAD has assumed its present form, held biennially in North America, alternating with its sister conference CHARME in Europe. We are delighted to report that our research community continues to flourish: we received 69 paper submissions, with many more high-quality papers than we had room to accept. After a rigorous review process, in which each paper received at least three, and typically four or more, independent reviews, we accepted 29 papers for the conference and inclusion in this volume. The conference also included invited talks from Greg Spirakis of Intel Corporation and Wayne Wolf of Princeton University. A conference of this size requires the contributions of numerous people. On the technical side, we are grateful to the program committee and the additional reviewers for their countless hours reviewing submissions and ensuring the intellectual quality of the conference. We would also like to thank the steering committee for their wisdom and guidance. On the logistical side, we thank Christa Mace for designing our website and attending to countless organizational tasks. And we thank our corporate sponsors – AMD, IBM, Intel, and Synopsys – for financial support that helped make this conference possible.