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Nota di contenuto	Invited Contributions -- View from the Fringe of the Fringe -- Hardware Synthesis Using SAFL and Application to Processor Design -- FMCAD 2000 -- Applications of Hierarchical Verification in Model Checking -- Model Checking 1 -- Pruning Techniques for the SAT-Based Bounded Model Checking Problem -- Heuristics for Hierarchical Partitioning with Application to Model Checking -- Short Papers 1 -- Efficient Reachability Analysis and Refinement Checking of Timed Automata Using BDDs -- Deriving Real-Time Programs from Duration Calculus Specifications -- Reproducing Synchronization Bugs with Model Checking -- Formally-Based Design Evaluation -- Clocking

Issues -- Multiclock Esterel -- Register Transformations with Multiple Clock Domains -- Temporal Properties of Self-Timed Rings -- Short Papers 2 -- Coverability Analysis Using Symbolic Model Checking -- Specifying Hardware Timing with ET-Lotos -- Formal Pipeline Design -- Verification of Basic Block Schedules Using RTL Transformations -- Joint Session with TPHOLs -- Parameterized Verification of the FLASH Cache Coherence Protocol by Compositional Model Checking -- Proof Engineering in the Large: Formal Verification of Pentium®4 Floating-Point Divider -- Hardware Compilation -- Towards Provably-Correct Hardware Compilation Tools Based on Pass Separation Techniques -- A Higher-Level Language for Hardware Synthesis -- Tools -- Hierarchical Verification Using an MDG-HOL Hybrid Tool -- Exploiting Transition Locality in Automatic Verification -- Efficient Debugging in a Formal Verification Environment -- Model Checking 2 -- Using Combinatorial Optimization Methods for Quantification Scheduling -- Net Reductions for LTL Model-Checking -- Component Verification -- Formal Verification of the VAMP Floating Point Unit -- A Specification Methodology by a Collection of Compact Properties as Applied to the Intel® Itanium™ Processor Bus Protocol -- The Design and Verification of a Sorter Core -- Case Studies -- Refinement-Based Formal Verification of Asynchronous Wrappers for Independently Clocked Domains in Systems on Chip -- Using Abstract Specifications to Verify PowerPC™ Custom Memories by Symbolic Trajectory Evaluation -- Algorithm Verification -- Formal Verification of Conflict Detection Algorithms -- Induction-Oriented Formal Verification in Symmetric Interconnection Networks -- A Framework for Microprocessor Correctness Statements -- Duration Calculus -- From Operational Semantics to Denotational Semantics for Verilog -- Efficient Verification of a Class of Linear Hybrid Automata Using Linear Programming.

Sommario/riassunto

This volume contains the proceedings of CHARME 2001, the Eleventh Advanced Research Working Conference on Correct Hardware Design and Veri?cation Methods. CHARME 2001 is the 11th in a series of working conferences devoted to the development and use of leading-edge formal techniques and tools for the design and veri?cation of hardware and hardware-like systems. Previous events in the ‘CHARME’ series were held in Bad Herrenalb (1999), Montreal (1997), Frankfurt (1995), Arles (1993), and Torino (1991). This series of meetings has been organized in cooperation with IFIP WG 10.5 and WG 10.2. Prior meetings, stretching backto the earliest days of formal hardware veri? cation, were held under various names in Miami (1990), Leuven (1989), Glasgow (1988), Grenoble (1986), Edinburgh (1985), and Darmstadt (1984). The convention is now well-established whereby the European CHARME conference alternates with its biennial counterpart, the International Conference on Formal Methods in Computer-Aided Design (FMCAD), which is held on even-numbered years in the USA. The conference tookplace during 4–7 September 2001 at the Institute for System Level Integration in Livingston, Scotland. It was co-hosted by the - stitute and the Department of Computing Science of Glasgow University and co-sponsored by the IFIP TC10/WG10.5 Working Group on Design and En- neering of Electronic Systems. CHARME 2001 also included a scienti?c session and social program held jointly with the 14th International Conference on Th- rem Proving in Higher Order Logics (TPHOLs), which was co-located in nearby Edinburgh.