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Nota di contenuto	Applications of Hierarchical Verification in Model Checking -- Applications of Hierarchical Verification in Model Checking -- Invited Talk -- Trends in Computing -- Invited Paper -- A Case Study in Formal Verification of Register-Transfer Logic with ACL2: The Floating Point Adder of the AMD Athlon TM Processor -- Contributed Papers -- An Algorithm for Strongly Connected Component Analysis in n log n Symbolic Steps -- Automated Refinement Checking for Asynchronous Processes -- Border-Block Triangular Form and Conjunction Schedule in Image Computation -- B2M: A Semantic Based Tool for BLIF Hardware Descriptions -- Checking Safety Properties Using Induction and a SAT-Solver -- Combining Stream-Based and State-Based Verification Techniques -- A Comparative Study of Symbolic Algorithms for the Computation of Fair Cycles -- Correctness of Pipelined Machines -- Do You Trust Your Model Checker? -- Executable Protocol Specification in ESL -- Formal Verification of Floating Point Trigonometric Functions -- Hardware Modeling Using Function Encapsulation -- A Methodology for the Formal Analysis of Asynchronous Micropipelines -- A Methodology for Large-Scale Hardware Verification -- Model Checking Synchronous Timing Diagrams -- Model Reductions and a Case Study -- Modeling and Parameters Synthesis for an Air TrafficManagement System -- Monitor-

Based Formal Specification of PCI -- SAT-Based Image Computation with Application in Reachability Analysis -- SAT-Based Verification without State Space Traversal -- Scalable Distributed On-the-Fly Symbolic Model Checking -- The Semantics of Verilog Using Transition System Combinators -- Sequential Equivalence Checking by Symbolic Simulation -- Speeding Up Image Computation by Using RTL Information -- Symbolic Checking of Signal-Transition Consistency for Verifying High-Level Designs -- Symbolic Simulation with Approximate Values -- A Theory of Consistency for Modular Synchronous Systems -- Verifying Transaction Ordering Properties in Unbounded Bus Networks through Combined Deductive/Algorithmic Methods -- Visualizing System Factorizations with Behavior Tables.

Sommario/riassunto

The biannual Formal Methods in Computer Aided Design conference (FMCAD 2000)is the third in a series of conferences under that title devoted to the use of discrete mathematical methods for the analysis of computer hardware and so- ware. The work reported in this book describes the use of modeling languages and their associated automated analysis tools to specify and verify computing systems. Functional veric ation has become one of the principal costs in a modern computer design e ort. In addition,verica tion of circuit models, timing,power, etc., requires even more eo rt. FMCAD provides a venue for academic and - dustrial researchers and practitioners to share their ideas and experiences of using discrete mathematical modeling and veric ation. It is noted with interest by the conference chairmen how this area has grown from just a few people 15 years ago to a vibrant area of research, development, and deployment. It is clear that these methods are helping reduce the cost of designing computing systems. As an example of this potential cost reduction, we have invited David Russino of Advanced Micro Devices, Inc. to describe his veric ation of ? oating-point - gorithms being used in AMD microprocessors. The program includes 30 regular presentations selected from 63 submitted papers.