1. Record Nr. UNINA9910451105403321

Autore	Simmel Georg <1858-1918., >
Titolo	The philosophy of money / / Georg Simmel ; edited by David Frisby ; translated by Tom Bottomore and David Frisby from a first draft by Kaethe Mengelberg
Pubbl/distr/stampa	London ; ; New York : , : Routledge, , 2004
ISBN	1-134-29439-5 0-203-69289-6 1-280-09873-2 0-203-48113-5
Edizione	[3rd enl. ed.]
Descrizione fisica	1 online resource (616 p.)
Altri autori (Persone)	BottomoreTom FrisbyDavid
Disciplina	332.4/01
Soggetti	Money Geld Electronic books.
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	"First published in 1978 by Routledge and Kegan Paul Ltd."--T.p. verso.
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Book Cover; Title; Contents; Acknowledgements; Note on the Translation; Preface to the Third Edition; Preface to the Second Edition; Introduction to the Translation; Preface; Value and Money; The Value of Money as a Substance; Money in the Sequence of Purposes; Individual Freedom; The Money Equivalent of Personal Values; The Style of Life; Afterword: The Constitution of the Text; Name Index;
Sommario/riassunto	This revised edition of the first complete translation of the seminal work 'Die Philosophie des Geldes' by Georg Simmel includes a new preface by David Frisby.

2. Record Nr. UNINA9910143489103321

Titolo	Field-Programmable Logic and Applications. From FPGAs to Computing Paradigm : 8th International Workshop, FPL'98 Tallinn, Estonia, August 31 - September 3, 1998 Proceedings / / edited by Reiner W. Hartenstein, Andres Keevallik
Pubbl/distr/stampa	Berlin, Heidelberg : , : Springer Berlin Heidelberg : , : Imprint : Springer, , 1998
ISBN	3-540-68066-7
Edizione	[1st ed. 1998.]
Descrizione fisica	1 online resource (XIII, 539 p.)
Collana	Lecture Notes in Computer Science, , 1611-3349 ; ; 1482
Disciplina	621.395
Soggetti	Computer systems Software engineering Artificial intelligence Logic design Computer arithmetic and logic units Computer hardware description languages Computer System Implementation Software Engineering Artificial Intelligence Logic Design Arithmetic and Logic Structures Register-Transfer-Level Implementation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di contenuto	New CAD framework extends simulation of dynamically reconfigurable logic -- Pebble: A language for parametrised and reconfigurable hardware design -- Integrated development environment for logic synthesis based on dynamically reconfigurable FPGAs -- Designing for Xilinx XC6200 FPGAs -- Perspectives of reconfigurable computing in research, industry and education -- Field-programmable logic: Catalyst for new computing paradigms -- Run-time management of dynamically reconfigurable designs -- Acceleration of satisfiability algorithms by

reconfigurable hardware -- An optimized design flow for fast FPGA-based rapid prototyping -- A knowledge-based system for prototyping on FPGAs -- JVX — A rapid prototyping system based on Java and FPGAs -- Prototyping new ILP architectures using FPGAs -- CAD system for ASM and FSM synthesis -- Fast floorplanning for FPGAs -- SRAM-based FPGAs: A fault model for the configurable logic modules -- Reconfigurable hardware as shared resource in multipurpose computers -- Reconfigurable computer array: The bridge between high speed sensors and low speed computing -- A reconfigurable engine for real-time video processing -- An FPGA implementation of a magnetic bearing controller for mechatronic applications -- Exploiting contemporary memory techniques in reconfigurable accelerators -- Self modifying circuitry — A platform for tractable virtual circuitry -- REACT: Reactive environment for runtime reconfiguration -- Evaluation of the XC6200-series architecture for cryptographic applications -- An FPGA-based object recognition machine -- PCI-SCI protocol translations: Applying microprogramming concepts to FPGAs -- Instruction-level parallelism for reconfigurable computing -- A hardware/software co-design environment for reconfigurable logic systems -- Mapping loops ontoreconfigurable architectures -- Speed optimization of the ALR circuit using an FPGA with embedded RAM: A design experience -- High-level synthesis for dynamically reconfigurable hardware/software systems -- Dynamic specialisation of XC6200 FPGAs by partial evaluation -- WebScope: A circuit debug tool -- Computing Goldbach partitions using pseudo-random bit generator operators on an FPGA systolic array -- Solving boolean satisfiability with dynamic hardware configurations -- Modular exponent realization on FPGAs -- Cost effective 2×2 inner product processors -- A field-programmable gate-array system for evolutionary computation -- A transmutable telecom system -- A survey of reconfigurable computing architectures -- A novel field programmable gate array architecture for high speed arithmetic processing -- Accelerating DTP with reconfigurable computing engines -- Hardware mapping of a parallel algorithm for matrix-vector multiplication overlapping communications and computations -- An interactive datasheet for the xilinx XC6200 -- Fast adaptive image processing in FPGAs using stack filters -- Increasing microprocessor performance with tightly-coupled reconfigurable logic arrays -- A high-performance computing module for a low earth orbit satellite using reconfigurable logic -- Maestro-link: A high performance interconnect for PC cluster -- A hardware implementation of Constraint Satisfaction Problem based on new reconfigurante LSI architecture -- A hardware operating system for dynamic reconfiguration of FPGAs -- High speed low level image processing on FPGAs using distributed arithmetic -- A flexible implementation of high-performance FIR filters on Xilinx FPGAs -- Implementing processor arrays on FPGAs -- Reconfigurable hardware — A study in codesign -- Statechart-based HW/SW-codesign of amulti-FPGA-board and a microprocessor -- Simulation of ATM switches using dynamically reconfigurable FPGA's -- Fast prototyping using system emulators -- Space-efficient mapping of 2D-DCT onto dynamically configurable coarse-grained architectures -- XILINX4000 architecture — Driven synthesis for speed -- The PLD-implementation of Boolean function characterized by minimum delay -- Reconfigurable PCI-BUS interface (RPCI) -- Programmable prototyping system for image processing -- A co-simulation concept for an efficient analysis of complex logic designs -- Programming and implementation of reconfigurable routers -- Virtual instruments based on reconfigurable logic -- The >S<puter: Introducing a novel concept for dispatching

	instructions using reconfigurable hardware -- A 6200 model and editor based on object technology -- Interfacing hardware and software -- Generating layouts for self-implementing modules.
Sommario/riassunto	This book constitutes the refereed proceedings of the 8th International Workshop on Field-Programmable Logics and Applications, FPL '98, held in Tallinn, Estonia, in August/September 1998. The 39 revised full papers presented were carefully selected for inclusion in the book from a total of 86 submissions. Also included are 30 refereed high-quality posters. The papers are organized in topical sections on design methods, general aspects, prototyping and simulation, development methods, accelerators, system architectures, hardware/software codesign, system development, algorithms on FPGAs, and applications.