1. Record Nr.	UNINA9910143467903321
Titolo	Formal methods in computer-aided design : second international conference, FMCAD '98, Palo Alto, CA, USA, November 4-6, 1998 : proceedings / / Ganesh Gopalakrishnan, Phillip Windley (editors)
Pubbl/distr/stampa	Berlin : , : Springer, , [1998] ©1998
ISBN	3-540-49519-3
Edizione	[1st ed. 1998.]
Descrizione fisica	1 online resource (X, 538 p.)
Collana	Lecture notes in computer science ; ; 1522
Disciplina	621.392
Soggetti	Digital integrated circuits - Computer-aided design Computer engineering - Computer-aided design Integrated circuits - Verification Automatic theorem proving Formal methods (Computer science)
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Minimalist Proof Assistants: Interactions of Technology and Methodology in Formal System Level Verification -- Reducing Manual Abstraction in Formal Verification of Out- of- Order Execution -- Bit-Level Abstraction in the Verification of Pipelined Microprocessors by Correspondence Checking -- Solving Bit-Vector Equations -- The Formal Design of 1M-Gate ASICs -- Design of Experiments for Evaluation of BDD Packages Using Controlled Circuit Mutations -- A Tutorial on Stålmarck's Proof Procedure for Propositional Logic -- Almana: A BDD Minimization Tool Integrating Heuristic and RewritingMethods -- Bisimulation Minimization in an Automata-Theoretic Verification Framework -- Automatic Verification of Mixed-Level Logic Circuits -- A Timed Automaton-Based Method for Accurate Computation of Circuit Delay in the Presence of Cross-Talk -- Maximum Time Separation of Events in Cyclic Systems with Linear and Latest Timing Constraints -- Using MTBDDs for Composition and Model Checking of Real-Time Systems -- Formal Methods in CAD from an Industrial Perspective -- A Methodology for Automated Verification of

Synthesized RTL Designs and Its Integration with a High-Level Synthesis Tool -- Combined Formal Post- and Presynthesis Verification in High Level Synthesis -- Formalization and Proof of a Solution to the PCI 2.1 Bus Transaction Ordering Problem -- A Performance Study of BDD-Based Model Checking -- Symbolic Model Checking Visualization -- Input Elimination and Abstraction in Model Checking -- Symbolic Simulation of the JEM1 Microprocessor -- Symbolic Simulation: An ACL2 Approach -- Verification of Data-Insensitive Circuits: An In-Order-Retirement Case Study -- Combining Symbolic Model Checking with Uninterpreted Functions for Out-of-Order Processor Verification -- Formally Verifying Data and Control with Weak Reachability Invariants -- Generalized Reversible Rules -- An Assume-Guarantee Rule for Checking Simulation -- Three Approaches to Hardware Verification: HOL, MDG, and VIS Compared -- An Instruction Set Process Calculus -- Techniques for Implicit State Enumeration of EFSMs -- Model Checking on Product Structures -- BDDNOW: A Parallel BDD Package -- Model Checking VHDL with CV -- Alexandria: A Tool for Hierarchical Verification -- PV: An Explicit Enumeration Model-Checker.

2.	Record Nr.	UNICAMPANIAVAN00123530
	Titolo	Eye Tracking and Visualization : Foundations, Techniques, and Applications. ETVIS 2015 / Michael Burch ... [et al.] editors
	Pubbl/distr/stampa	Cham, : Springer, 2017
	Titolo uniforme	Eye Tracking and Visualization : Foundations, Techniques, and Applications. ETVIS 2015
	Descrizione fisica	xii, 258 p. : ill. ; 24 cm
	Soggetti	62-XX - Statistics [MSC 2020]
		68-XX - Computer science [MSC 2020]
		68Uxx - Computing methodologies and applications [MSC 2020]
	Lingua di pubblicazione	Inglese
	Formato	Materiale a stampa
	Livello bibliografico	Monografia