1. Record Nr. UNISA996391002003316

Autore	D'Ewes Simonds, Sir, <1602-1650.>
Titolo	Two speeches spoken by Sir Simonds D'Ewes [[electronic resource]] : The first touching the antiquity of Cambridge, lately published by Iohn Thomas, with many ignorant and foolish mistakes which are here rectified. The other concerning the priviledge of Parliament in causes civill and criminall
Pubbl/distr/stampa	London, : Printed for Thomas Paybody, dwelling in Queenes Head Court in Pater-noster Row, 1642
Descrizione fisica	[2], 6 p
Soggetti	Great Britain Politics and government 1625-1649 Early works to 1800
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Composed of two speeches: Thomason E.196[24] has the caption title "A speech delivered in Parliament by Sir Simonds D'Ewes" on the first page of text. Thomason E.196[25] is "A speech spoken by Sir Simonds D'Ewes, (so neare as it could be collected together) touching the priviledge of Parliament in causes criminall and civill". Annotation on Thomason copy: "Jan: 2d 1640". Title page has printers' device (McK. 417). Reproduction of the original in the British Library.
Sommario/riassunto	eebo-0018

2. Record Nr. UNINA9910143460703321

Titolo	Computer-aided verification : 11th International Conference, Cav '99, Trento, Italy, July 6-1-10, 1999 : proceedings / / Nicolas Halbwachs, Doron Peled (editors)
Pubbl/distr/stampa	Berlin : , : Springer, , [1999] Â©1999
ISBN	3-540-48683-6
Edizione	[1st ed. 1999.]
Descrizione fisica	1 online resource (XIV, 506 p.)
Collana	Lecture notes in computer science ; ; 1633
Disciplina	005.14
Soggetti	Computer software - Verification Electronic digital computers - Evaluation
Lingua di pubblicazione	Inglese
Formato	Materiale a stampa
Livello bibliografico	Monografia
Note generali	Bibliographic Level Mode of Issuance: Monograph
Nota di bibliografia	Includes bibliographical references and index.
Nota di contenuto	Tutorials and Invited Papers -- Alternative Approaches to Hardware Verification -- The Compositional Specification of Timed Systems — A Tutorial -- Timed Automata -- Ståalmarck's Method with Extensions to Quantified Boolean Formulas -- Verification of Parameterized Systems by Dynamic Induction -- Formal Methods for Conformance Testing: Theory Can Be Practical -- Processor Verification -- Proof of Correctness of a Processor with Reorder Buffer Using the Completion Functions Approach -- Verifying Safety Properties of a PowerPC? Microprocessor Using Symbolic Model Checking without BDDs -- Model Checking the IBM Gigahertz Processor: An Abstraction Algorithm for High-Performance Netlists -- Validation of Pipelined Processor Designs Using Esterel Tools: A Case Study -- Protocol Verification and Testing -- Automated Verification of a Parametric Real-Time Program: The ABR Conformance Protocol -- Test Generation Derived from Model-Checking -- Latency Insensitive Protocols -- Infinite State Space -- Handling Global Conditions in Parametrized System Verification -- Verification of Infinite-State Systems by Combining Abstraction and Reachability Analysis -- Experience with Predicate Abstraction -- Theory of Verification -- Model Checking of Safety Properties -- A Complete Finite Prefix for Process Algebra -- The Mathematical Foundation of Symbolic Trajectory Evaluation -- Assume-Guarantee

Refinement between Different Time Scales -- Linear Temporal Logic -- Efficient Decision Procedures for Model Checking of Linear Time Logic Properties -- Stutter-Invariant Languages, ?-Automata, and Temporal Logic -- Improved Automata Generation for Linear Temporal Logic -- Modeling of Systems -- On the Representation of Probabilities over Structured Domains -- Model Checking Partial State Spaces with 3-Valued Temporal Logics -- Elementary Microarchitecture Algebra -- Verifying Sequential Consistency on Shared-Memory Multiprocessor Systems -- Symbolic Model-Checking -- Stepwise CTL Model Checking of State/Event Systems -- Optimizing Symbolic Model Checking for Constraint-Rich Models -- Efficient Timed Reachability Analysis Using Clock Difference Diagrams -- Theorem Proving -- Mechanizing Proofs of Computation Equivalence -- Linking Theorem Proving and Model-Checking with Well-Founded Bisimulation -- Automatic Verification of Combinational and Pipelined FFT Circuits -- Automata-Theoretic Methods -- Efficient Analysis of Cyclic Definitions -- A Theory of Restrictions for Logics and Automata -- Model Checking Based on Sequential ATPG -- Automatic Verification of Abstract State Machines -- Abstraction -- Abstract and Model Check while You Prove -- Deciding Equality Formulas by Small Domains Instantiations -- Exploiting Positive Equality in a Logic of Equality with Uninterpreted Functions -- Tool Presentations -- A Toolbox for the Analysis of Discrete Event Dynamic Systems -- TIPPtool: Compositional Specification and Analysis of Markovian Performance Models -- Java Bytecode Verification by Model Checking -- NuSMV: A New Symbolic Model Verifier -- PIL/SETHEO: A Tool for the Automatic Analysis of Authentication Protocols.

Sommario/riassunto

This book constitutes the refereed proceedings of the 11th International Conference on Computer Aided Verification, CAV'99, held in Trento, Italy in July 1999 as part of FLoC'99. The 34 revised full papers presented were carefully reviewed and selected from a total of 107 submissions. Also included are six invited contributions and five tool presentations. The book is organized in topical sections on processor verification, protocol verification and testing, infinite state spaces, theory of verification, linear temporal logic, modeling of systems, symbolic model checking, theorem proving, automata-theoretic methods, and abstraction.