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Nota di contenuto	ALL-DIGITAL FREQUENCY SYNTHESIZER IN DEEP-SUBMICRON CMOS; CONTENTS; PREFACE; Acknowledgments; 1 INTRODUCTION; 1.1 Frequency Synthesis; 1.1.1 Noise in Oscillators; 1.1.2 Frequency Synthesis Techniques; 1.2 Frequency Synthesizer as an Integral Part of an RF Transceiver; 1.2.1 Transmitter; 1.2.2 Receiver; 1.2.3 Toward Direct Transmitter Modulation; 1.3 Frequency Synthesizers for Mobile Communications; 1.3.1 Integer-N PLL Architecture; 1.3.2 Fractional-N PLL Architecture; 1.3.3 Toward an All-Digital PLL Approach; 1.4 Implementation of an RF Synthesizer 1.4.1 CMOS vs. Traditional RF Process Technologies 1.4.2 Deep-Submicron CMOS; 1.4.3 Digitally Intensive Approach; 1.4.4 System Integration; 1.4.5 System Integration Challenges for Deep-Submicron CMOS; 2 DIGITALLY CONTROLLED OSCILLATOR; 2.1 Varactor in a Deep-Submicron CMOS Process; 2.2 Fully Digital Control of Oscillating

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3.4 Principle of Synchronously Optimal DCO Tuning Word Retiming; 3.5 Time Dithering of DCO Tuning Input; 3.5.1 Oscillator Tune Time Dithering Principle; 3.5.2 Direct Time Dithering of Tuning Input; 3.5.3 Update Clock Dithering Scheme; 3.6 Implementation of PVT and Acquisition DCO Bits; 3.7 Implementation of Tracking DCO Bits; 3.7.1 High-Speed Dithering of Fractional Varactors; 3.7.2 Dynamic Element Matching of Varactors; 3.7.3 DCO Varactor Rearrangement; 3.8 Time-Domain Model; 3.9 Summary; 4 ALL-DIGITAL PHASE-LOCKED LOOP; 4.1 Phase-Domain Operation
4.2 Reference Clock Retiming
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4.14 Nonlinear Differential Term of an ADPLL

Sommario/riassunto

A new and innovative paradigm for RF frequency synthesis and wireless transmitter design Learn the techniques for designing and implementing an all-digital RF frequency synthesizer. In contrast to traditional RF techniques, this innovative book sets forth digitally intensive design techniques that lead the way to the development of low-cost, low-power, and highly integrated circuits for RF functions in deep submicron CMOS processes. Furthermore, the authors demonstrate how the architecture enables readers to integrate an RF front-end with the digital back-end onto a single silicon die
