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Nota di contenuto	MODERN RECEIVER FRONT-ENDS; CONTENTS; Preface; Acknowledgments; 1 INTRODUCTION; 1.1 Current State of the Art; 2 RECEIVER SYSTEM DESIGN; 2.1 Frequency Planning; 2.1.1 Blockers; 2.1.2 Spurs and Desensing; 2.1.3 Transmitter Leakage; 2.1.4 LO Leakage and Interference; 2.1.5 Image; 2.1.6 Half IF; 2.2 Link Budget Analysis; 2.2.1 Linearity; 2.2.2 Noise; 2.2.3 Signal-to-Noise Ratio; 2.2.4 Receiver Gain; 2.3 Propagation Effects; 2.3.1 Path Loss; 2.3.2 Multipath and Fading; 2.3.3 Equalization; 2.3.4 Diversity; 2.3.5 Coding; 2.4 Interface Planning; 2.5 Conclusion; 3 REVIEW OF RECEIVER ARCHITECTURES 3.1 Heterodyne Receivers 3.2 Image Reject Receivers; 3.2.1 Hartley Architecture; 3.2.2 Weaver Architecture; 3.3 Zero IF Receivers; 3.4 Low IF Receivers; 3.5 Issues in Direct Conversion Receivers; 3.5.1 Noise; 3.5.2 LO Leakage and Radiation; 3.5.3 Phase and Amplitude Imbalance; 3.5.4 DC Offset; 3.5.5 Intermodulations; 3.6 Architecture Comparison and Trade-off; 3.7 Conclusion; 4 SILICON-BASED RECEIVER DESIGN; 4.1 Receiver Architecture and Design; 4.1.1 System Description and

Calculations; 4.1.2 Basics of OFDM; 4.1.3 System Architectures; 4.1.4 System Calculations; 4.2 Circuit Design  
4.2.1 SiGe BiCMOS Process Technology; 4.2.2 LNA; 4.2.3 Mixer; 4.2.4 Frequency Divider; 4.3 Receiver Design Steps; 4.3.1 Design and Integration of Building Blocks; 4.3.2 DC Conditions; 4.3.3 Scattering Parameters; 4.3.4 Small-Signal Performance; 4.3.5 Transient Performance; 4.3.6 Noise Performance; 4.3.7 Linearity Performance; 4.3.8 Parasitic Effects; 4.3.9 Process Variation; 4.3.10 50-W and Non-50-W Receivers; 4.4 Layout Considerations; 4.5 Characterization of Receiver Front-Ends; 4.5.1 DC Test; 4.5.2 Functionality Test; 4.5.3 S-Parameter Test; 4.5.4 Conversion Gain Test; 4.5.5 Linearity Test; 4.5.6 Noise Figure Test; 4.5.7 I/Q Imbalance; 4.5.8 DC Offset; 4.6 Measurement Results and Discussions; 4.6.1 Close Examination of Noise Figure and I/Q Imbalance; 4.6.2 Comments on I/Q Imbalance; 4.7 Conclusion; 5 SUBHARMONIC RECEIVER DESIGNS; 5.1 Illustration of Subharmonic Techniques; 5.2 Mixing Using Antisymmetric I-V Characteristics; 5.3 Impact of Mismatch Effects; 5.4 DC Offset Cancellation Mechanisms; 5.4.1 Intrinsic DC Offset Cancellation; 5.4.2 Extrinsic DC Offset Cancellation; 5.5 Experimental Verification of DC Offset; 5.6 Waveform Shaping Before Mixing; 5.6.1 Theory and Analysis; 5.6.2 Experimental Verification on GaAs MESFET APDP; 5.6.3 Implementation in Silicon; 5.7 Design Steps for APDP-Based Receivers; 5.8 Architectural Illustration; 5.9 Fully Monolithic Receiver Design Using Passive APDP Cores; 5.9.1 Integrated Direct Conversion Receiver MMIC's; 5.9.2 Receiver Blocks; 5.9.3 Additional Receiver Blocks; 5.10 Reconfigurable Multiband Subharmonic Front-Ends; 5.11 Conclusion; 6 ACTIVE SUBHARMONIC RECEIVER DESIGNS; 6.1 Stacking of Switching Cores; 6.1.1 Description and Principles; 6.1.2 Subharmonic Receiver Architecture; 6.2 Parallel Transistor Stacks; 6.2.1 Active Mixer; 6.2.2 Receiver Architecture

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Architectures BABAK MATINPOUR and JOY LASKAR\* Describes the actual implementation of receiver architectures from the initial design to an IC-based product\* Presents many tricks-of-the-trade not usually covered in textbooks\* Covers a range of practical issues including semiconductor technology selection, cost versus performance, yield, packaging, prototype development, testing, and analysis\* Discusses architectures that are employed in modern broadband wireless systems

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