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Nota di contenuto	Simulation-based functional test generation for embedded processors," C. -- Scalable defect mapping and configuration of memory-based nanofabrics,"Chen -- Improvement of fault injection techniques based on VHDL code modification,"J. -- MVP: a mutation-based validation paradigm,"J. -- Establishing latch correspondence for embedded circuits of PowerPC microprocessors,"H. -- Sequential equivalence checking based on k-th invariants and circuit SAT solving,"Feng -- VERISEC: verifying equivalence of sequential circuits using SAT,"M. -- Automated clock inference for stream function-based system level specifications,"J. -- Cosimulation of ITRON-based embedded software with SystemC,"S. -- A software test program generator for verifying system-on-chips,"A. -- Stimulus generation for interface protocol verification using the nondeterministic extended finite state machine model,"Che-Hua -- DVGen: a test generator for the transmeta Efficeon VLIW processor,"K. -- Reuse in system-level stimuli-generation,"Y. -- Harnessing machine learning to improve the success rate of stimuli generation,"S. -- A new simulation-based property checking algorithm based on partitioned alternative search space traversal,"Qingwei -- Validating families of latency insensitive protocols,"S. -- GASIM: a fast Galois field based simulator for functional model,"D. -- Overlap reduction in symbolic system traversal,"P. -- Formal verification of high-level conformance with symbolic simulation,"R. -- A method for generation of GSTE assertion graphs,"E. -- Automatic abstraction

refinement for Petri nets verification,"Zhenyu -- An optimum algorithm for compacting error traces for efficient functional debugging,"Chia-Chih -- Increasing the deducibility in CNF instances for efficient SAT-based bounded model checking,"V. -- B-cubing theory: new possibilities for efficient SAT-solving,"D. -- Multilevel design validation in a secure embedded system,"D. -- Security evaluation against electromagnetic analysis at design time,"Huiyun -- Formal meaning of coverage metrics in simulation-based hardware design verification,"I. -- Advanced analysis techniques for cross-product coverage,"H. -- A proof of correctness for the construction of property monitors,".