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Nota di contenuto	Title page; Copyright page; Contents; Preface; Contributors; 1: Low Power Multicore Processors for Embedded Systems; 1.1 Multicore Chip with Highly Efficient Cores; 1.2 SuperHTM RISC Engine Family (SH) Processor Cores; 1.2.1 History of SH Processor Cores; 1.2.2 Highly Efficient ISA; 1.2.3 Asymmetric In-Order Dual-Issue Superscalar Architecture; 1.3 SH-X: A Highly Efficient CPU Core; 1.3.1 Microarchitecture Selections; 1.3.2 Improved Superpipeline Structure; 1.3.3 Branch Prediction and Out-of-Order Branch Issue; 1.3.4 Low Power Technologies; 1.3.5 Performance and Efficiency Evaluations 1.4 SH-X FPU: A Highly Efficient FPU1.4.1 FPU Architecture of SH Processors; 1.4.2 Implementation of SH-X FPU; 1.4.3 Performance Evaluations with 3D Graphics Benchmark; 1.5 SH-X2: Frequency and Efficiency Enhanced Core; 1.5.1 Frequency Enhancement; 1.5.2 Low Power Technologies; 1.6 SH-X3: Multicore Architecture Extension; 1.6.1 SH-X3 Core Specifications; 1.6.2 Symmetric and Asymmetric Multiprocessor Support; 1.6.3 Core Snoop Sequence Optimization; 1.6.4 Dynamic Power Management; 1.6.5 RP-1 Prototype Chip; 1.6.6 RP-2 Prototype Chip; 1.7 SH-X4: ISA and Address Space Extension 1.7.1 SH-X4 Core Specifications1.7.2 Efficient ISA Extension; 1.7.3 Address Space Extension; 1.7.4 Data Transfer Unit; 1.7.5 RP-X Prototype Chip; References; 2: Special-Purpose Hardware for Computational Biology; 2.1 Molecular Dynamics Simulations on

Graphics Processing Units; 2.1.1 Molecular Mechanics Force Fields; 2.1.2 Graphics Processing Units for MD Simulations; 2.2 Special-Purpose Hardware and Network Topologies for MD Simulations; 2.2.1 High-Throughput Interaction Subsystem; 2.2.2 Hardware Description of the Flexible Subsystem; 2.2.3 Performance and Conclusions  
2.3 Quantum MC Applications on Field-Programmable Gate Arrays  
2.3.1 Energy Computation and WF Kernels; 2.3.2 Hardware Architecture; 2.3.3 PE and WF Computation Kernels; 2.4 Conclusions and Future Directions; References; 3: Embedded GPU Design; 3.1 Introduction; 3.2 System Architecture; 3.3 Graphics Modules Design; 3.3.1 RISC Processor; 3.3.2 Geometry Processor; 3.3.3 Rendering Engine; 3.4 System Power Management; 3.4.1 Multiple Power-Domain Management; 3.4.2 Power Management Unit; 3.5 Implementation Results; 3.5.1 Chip Implementation; 3.5.2 Comparisons; 3.6 Conclusion; References  
4: Low-Cost VLSI Architecture for Random Block-Based Access of Pixels in Modern Image Sensors  
4.1 Introduction; 4.2 The DVP Interface; 4.3 The iBRIDGE-BB Architecture; 4.3.1 Configuring the iBRIDGE-BB; 4.3.2 Operation of the iBRIDGE-BB; 4.3.3 Description of Internal Blocks; 4.4 Hardware Implementation; 4.4.1 Verification in Field-Programmable Gate Array; 4.4.2 Application in Image Compression; 4.4.3 Application-Specific Integrated Circuit (ASIC) Synthesis and Performance Analysis; 4.5 Conclusion; Acknowledgments; References; 5: Embedded Computing Systems on FPGAs; 5.1 FPGA Architecture  
5.2 FPGA Configuration Technology

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## Sommario/riassunto

"The book begins with an introduction of embedded computing systems, honing in on system on a chip (SoCs), multi-processor System-on-Chip (MPSoCs) and Network operation centers (NoCs). It covers on-chip integration of software and custom hardware accelerators, as well as fabric flexibility, custom architectures, and the multiple I/O standards that facilitate PCB integration. The second portion of the book focuses on the technologies associated with embedded computing systems. It also covers the basics of field-programmable gate array (FPGA), digital signal processing (DSP) and application-specific integrated circuit (ASIC) technology, architectural support for on-chip integration of custom accelerators with processors and O/S support for these systems. The third area focuses on architecture, testability and computer-aided design (CAD) support for embedded systems, soft processors, heterogeneous resources, on-chip storage. The final section covers software support, in particular O/S (linux, research and technology organization (RTO))"--

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