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Properties; 2.5 Limit/Issues with the Porogen Approach; 2.5.1 Porosity Creation Limit; 2.5.2 Porogen Residues; 2.6 Future of CVD Low-k
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3.5.4 Effect of Photon Energy and Intensity 3.5.5 Plasma Damage by Oxidative Radicals; 3.5.6 Hydrogen-Based Plasma; 3.5.7 Minimization of Plasma Damage; 3.6 Dielectric Recovery; 3.6.1 CH₄ Beam Treatment; 3.6.2 Dielectric Recovery by Silylation; 3.6.3 UV Radiation; 3.7 Conclusions; References; 4 Wet Clean Applications in Porous Low-k Patterning Processes; 4.1 Introduction; 4.2 Silica and Porous Hybrid Dielectric Materials; 4.3 Impact of Plasma and Subsequent Wet Clean Processes on the Stability of Porous Low-k Dielectrics; 4.3.1 Stability in Pure Chemical Solutions
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5.3.3 The Role of Leveler

Sommario/riassunto

Finding new materials for copper/low-k interconnects is critical to the continuing development of computer chips. While copper/low-k interconnects have served well, allowing for the creation of Ultra Large Scale Integration (ULSI) devices which combine over a billion transistors onto a single chip, the increased resistance and RC-delay at the smaller scale has become a significant factor affecting chip performance. Advanced Interconnects for ULSI Technology is dedicated to the materials and methods which might be suitable replacements. It covers a broad range of topics, from physical
