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Nota di contenuto	Foreword -- Organizing Committee -- Program Committee -- Steering Committee -- Reviewers -- Acknowledgements -- Test Technology Technical Council (TTTC) -- Test Technology Educational Program (TTEP) Tutorials -- Awards -- Session 1 Session 1A: Post-Silicon Debug & Customer returns -- Session 1B: 3D ICS -- IP Session 1C: Test and Characterization of High-Speed Circuits -- Session 2 Session 2A: Power Issues in Test -- Session 2B: Analog, Mixed-Signal & RF Test/Diagnosis -- IP Session 2C: On Chip Parametric Sensors -- Session 3 Session 3A: Delay & Performance Test 1 -- Special Session 3B: Hot Topic: Multifaceted Approaches for Field Reliability -- IP Session 3C: Advanced Methods for Leveraging New Test Standards -- Session 4 Special Session 4A: New Topics -- Session 4B: Panel: Security -- IP Session 4C: The Buck Stops With Wafer Test: Dream Or Reality? -- Session 5 Special Session 5A: Apprentice, Season 4 -- Special Session 5B: Panel: How Much Toggle Activity Should We Be Testing With? -- Session 6 Session 6A: Delay & Performance Test 2 -- Session 6B: Memory Test and Repair -- IP Session 6C: The Bang For The Buck With Resiliency: Yield Or Field? -- Session 7 Session 7A: Low-Power IC Test -- Session 7B: On-line & System Testing -- Session 8 Session 8A: Aging, Transients & Soft Errors -- Special Session 8B: New Topic: Solar Cells -- Sessions 9 Special Session 9C: Panel: Coverage Closure in SoC Verification: Are We Chasing a Mirage? -- Session 10 Session 10A: Design for Testability 1 -- Session 10B: Error & Fault Tolerance 1 -- Session 11 Session 11A: Design for Testability 2 -- Session 11B: Error & Fault Tolerance 2 -- Session 12 Session 12A: ATPG & Compression -- Session 12B:

Reducing Test & Diagnosis Costs -- Session 13 Special Session 13A: Practical Signal Processing at Mixed Signal Test Venues - Trend Removal, Noise Reduction, Wideband Signal Capturing -- Session 13B: Hot Topic: Smart Silicon -- Session 13C: Hot Topic: Design and Test of 3D and Emerging Memories.